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RADC-TR-81-97
Interim Report
July 1981

LEVEL II

IRCCD FENCE SENSOR SYSTEM

RCA Government Systems Division

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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Assembly and wiring of the first advanced development model, ADM-1, was completed and checked out, and examination of system noise using an electrically inputted CCD was performed. Several dewars were assembled and tested, and a number of cooldown tests using the 1-W split-cycle coolers were performed. Some preliminary system data in the IR imaging mode was obtained and optical focusing of the array was accomplished. Wiring of the ADM-2 sensor unit was completed as was a portion of the

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mechanical assembly. An eighth system board, the EPROM expansion board, needed for a parameter change in ADMs 2 to 5, was designed, a hand-wired version was assembled and partially tested, and the wiring of the laboratory system was revised to accommodate the EPROM expansion board.

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Section I

INTRODUCTION AND SUMMARY

This report, covering the period 1 June 1980 through 30 November 1980, is the third interim report of the IRCCD Fence Sensor Program and deals with the assembly and checkout of the first advanced development model (ADM-1), evaluation of the subassemblies of ADM-1 (including sensor electronics, signal processor, dewars and coolers), checkout of ADM-1 using a room-temperature electrically inputted CCD to simulate targets, and evaluation of ADM-1 with a CCD cooled by a one-watt split cycle cooler and viewing a laboratory background.

ADM-1 was originally configured with a hard vacuum dewar in the sensor unit similar in concept and design to the tri-services common module dewar. Progress made toward the development of such a dewar is described in this report and includes problems and fixes relating to dewar assembly, and approaches to the cooler cold finger-to-dewar top cap thermal interface.

Summaries of accomplishments in each major functional area are given below.

- Sensor Electronics - The ADM-1 chassis was wired and checked out. Debugging of ADM-1 and interfacing and checkout of ADM-1 with the computer was performed using an electrically inputted CCD operating at room temperature and two EPROM sets, sets 5 and 6. A number of approaches to reducing computer- and cooler compressor-induced noise in ADM-1 were tried and evaluated. Limited operation in the IR mode was realized using a CCD (TC1258-1-B-3-23) cooled with a number of 1-W split-cycle coolers in a sealed vacuum dewar, the ADM-1B dewar. Attempts to operate in the IR mode revealed deficiencies in both the dewar and in the coolers which precluded attaining sufficiently low temperature except for a few brief periods. The final printed circuit board required for ADM-1 (the system support board) was fabricated and checked out. Wiring of the ADM-2 chassis was completed and an eighth board required for ADM-2, an EPROM expansion board, was designed and a wire-wrap version of the board was checked out.

- Signal Processor - Testing of the software used in ADM-1 (contained in EPROM set 6) has revealed the need for revisions in the threshold determination routine. The variable gain introduced by the ALC subsystem was not correctly factored into the threshold decision algorithm. The corrected algorithm required the decision threshold for all 256 sensors to be updated after any integration mode change. An algorithm was developed specifically for the threshold update to minimize the execution time required for this task. The algorithm makes use of the previous threshold to limit the number of searches required to determine the update threshold. A background time

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average saturation test was added to the sensor update algorithm. It eliminates alarms due to hot scene artifacts and saturated sensors upon integration mode change.

- Dewar - Several modifications were made in dewar assembly to avoid mechanical reliability problems encountered with the glass wagonwheel feedthrough. A dewar using indium solder to join the dewar stainless steel outer wall to the Kovar section of the wagonwheel feedthrough and coated with a vacuum sealant around the solder joint was assembled. This dewar, designated the ADM-1B dewar, contained the first potentially operable IRCCD to survive the dewar assembly procedure. Liquid nitrogen boiloff tests performed to measure the dewar heat load indicate that it is about 520 mW. The temperature drop across the cooler cold tip to the dewar top cap (to which the CCD package is soldered) was measured to be $6^{\circ}K$ for a standard fuzz button/air interface.

- Coolers - The five, 1-W split-cycle coolers ordered for the program (coolers S/N 009, 011, 012, 013 and 014) were received and each cooler has been operated. Three of the coolers (009, 011 and 013) have been returned to the manufacturer for rework and/or examination.

The second interim report presented progress during the period from the critical design review (CDR) 28 November 1979 through 30 June 1980 when assembly of the first advanced development model, ADM-1 was initiated. The major activity during this period was the development of the subsystems that will be integrated into the deliverable equipment. Specific accomplishments by major functional area were:

- Sensor Electronics - Six of the seven printed circuit boards required for the ADM-1 sensor unit were fabricated.

- Signal Processor - The single-board computers, Texas Instruments TMS990/101, were purchased and the code necessary to implement the Purdue algorithm and an intruder classifier was written.

- Dewar - A test dewar employing all the materials, components, and assembly procedures to be used in the deliverable equipment was assembled.

- Cooler - The first cooler was accepted at the manufacturer's facilities (Martin-Marietta, Orlando, FLA.).

- Optics - All the lenses (developed by Research Optical Systems), cold filters (produced by OCLI) and AR-coated sapphire windows were procured and cold shields were fabricated.

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- **Mechanical and Packaging** - Sheet metal parts (for example, pc board nest, baseplate, and power supply brackets) required for chassis wiring were fabricated along with the optical mounting and alignment fixtures; a purchase order was placed (with the Zero Corp.) for the cases which constitute the ADM package.

- **Power Conditioning** - Power supplies and regulators were purchased and checked.

- **Miscellaneous** - Cooling fans, cables, connectors, and RFI/EMI filters were purchased.

The first interim report on this program covered the period from the beginning of the contract, 12 March 1979, through the CDR. Activity during that period was divided into two broad phases. The first phase ended with the preliminary design review (PDR), 10 July 1979, and the second with the CDR. Prior to the PDR the system design was refined and tradeoffs were made in each of the major functional areas (for example, microprocessor selection and cooler selection). Between the PDR and the CDR, decisions taken at the PDR were implemented, purchase orders for long-lead items were placed, and detailed designs were begun or, in some cases, continued.

Section II

ADM ASSEMBLY

The arrangement of the major ADM-1 assemblies, sensor unit, data/power interconnect cable, interface box, and video terminal is shown in Fig. 1. A simplified block diagram of the ADM-1 sensor unit electronics is given in Fig. 2. An additional printed circuit board, an EPROM expansion board not shown in Fig. 2, will be used in ADMs 2 to 5 to allow them to incorporate a parameter change feature not present in ADM-1.

During the period covered by this report, wiring of the ADM-1 and ADM-2 sensor units was completed. Operation of the ADM-1 system (sensor unit, interface box, video terminal, a Lear Siegler ADM-42, and data/power interconnect cable) was checked out. System checkout, to date, has consisted almost entirely of operating the system using the output of a room temperature electrically inputted CCD to generate targets of various widths and amplitudes. The signal output is operated upon by the analog signal conditioning circuit of the sensor unit, and then by the sensor unit's analog-to-digital converter and computer.

Most of the circuitry and hardware which make up an ADM system have been described in the Second Interim Report.[1] Those portions of the circuitry not previously described will be covered here. They include the power conditioning and control circuitry of the sensor unit, the interface box, and the data/power system interconnect cable. In addition, a description will also be given of the EPROM expansion board being developed for ADMs 2 to 5.

A. POWER CONDITIONING AND CONTROL

The power conditioning and control circuitry of the sensor unit is shown in Fig. 3. The components contained within the dashed lines are located on the system support and CCD bias boards, but are illustrated here because of their relevance to the power conditioning and control circuitry. Components associated with the power conditioning and control circuitry include an RFI/EMI enclosure, 3 Airpax 07A312BC1 DPST relays, 2 Elmwood thermostats — a high-temperature shutdown 80108 and a low-temperature shutdown 80106, an Airpax AP-12-8-5-2F-502 DPST circuit breaker, a Rotron Sparton RT-1174D°F fan, a Logitek DMN2A1HIS time delay unit, an Abbott CD5.0 +5-V switching power supply, an Abbott CC15D1.0 ±15-V switching power supply, an LM140K-12 +12-V regulator, an LM120K-12 -12-V regulator, and an MJ4032 power transistor.

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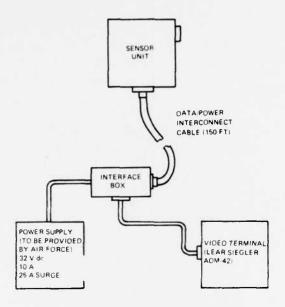
Fig. 1.   Arrangement of the ADM-1 system major assemblies.
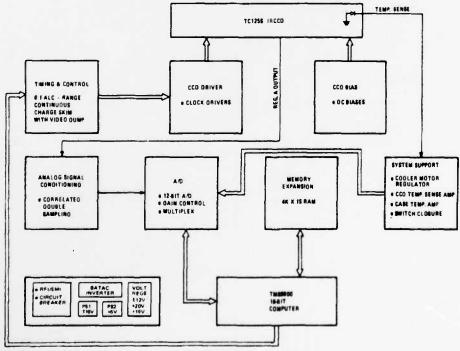
Fig. 2.   Sensor Unit electronics block diagram (ADM-1).

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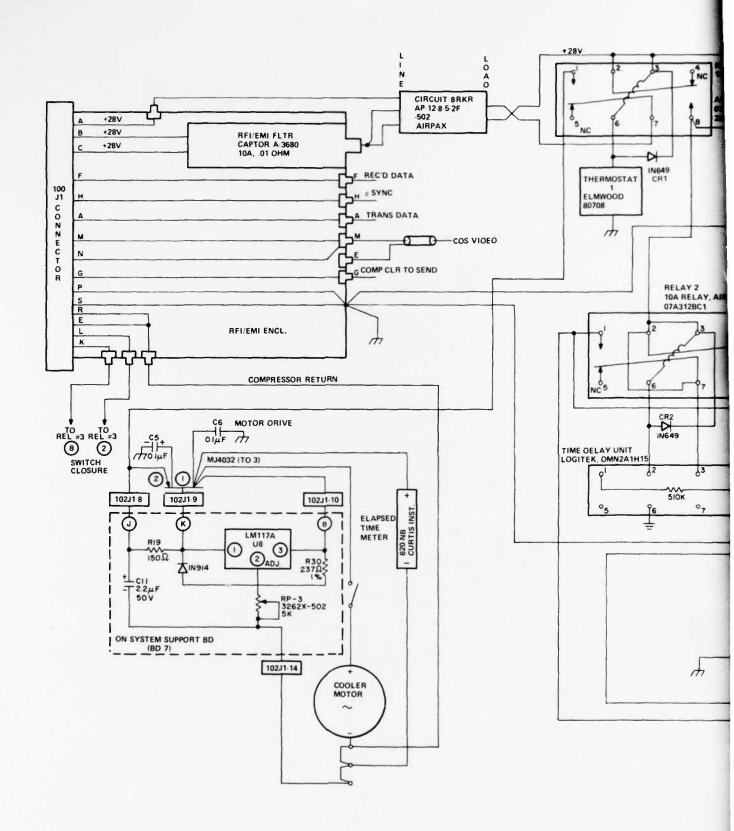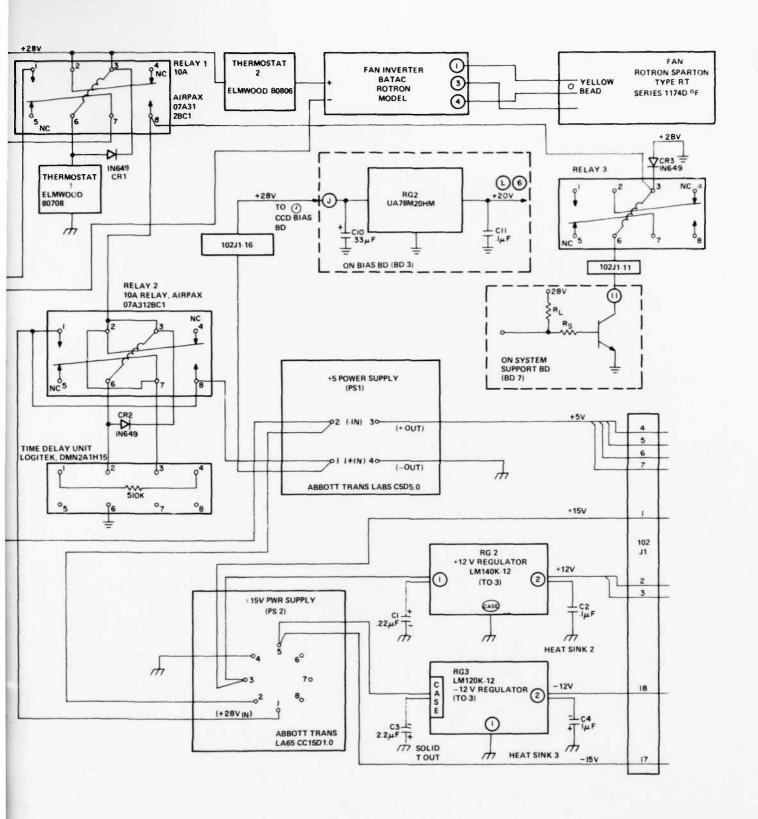
Fig. 3. Power conditioning and control circuitry.

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All power/signal lines entering or leaving the sensor unit pass through the RFI/EMI enclosure to reduce electrical interference from the sensor unit electronics. The RFI/EMI enclosure (shown in Fig. 4) contains a Bendix JT07-RE-20-16P (014) connector that engages to the data/power cable (a 150-ft system interconnect cable), a Captor A-2680 0.01-ohm RFI/EMI power line filter, six Erie 1201-052 bulkhead feedthrough RFI/EMI filters, and 5-Omni Spectra 2004-7188-02 bulkhead feedthroughs, which act as high-frequency cutoff, low-pass filters.

The dc power (30 V at the input to the sensor unit) enters via the Bendix connector on three lines, two of which pass through the Captor filter in the RFI/EMI enclosure. The output of this filter is connected to one arm of the Airpax circuit breaker. The third power line is connected to an Erie RFI/EMI filter, the output of which is connected to the second arm of the circuit breaker. Three power return lines pass through the RFI/EMI enclosure with two being grounded to the chassis of the sensor unit. The third power return line is the ground of the cooler compressor and it is returned to the ground-based interface box. This is to isolate the signal conditioning circuits in the sensor electronics from the current and voltage noise produced by the cooler compressor. The compressor return line enters the RFI/EMI box via an Erie filter.

The two outputs of the circuit breaker are connected to the two input arms of of Relay 1. The 80108 high temperature shutdown thermostat, used in series with
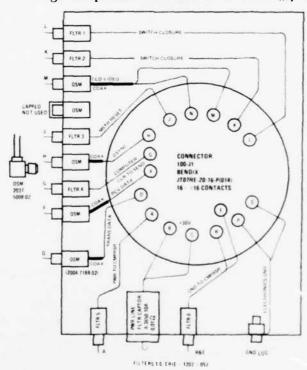
Fig. 4. Wiring arrangement of RFI/EMI enclosure.

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the relay coil, causes the relay to dropout if a temperature above 75°C is sensed. This thermostat is mounted on an edge of the power supply heatsink below the 5-V power supply. If the temperature rises above 75°C, all system power is turned off except for power to the BATAC-driven cooling fan which is supplied directly from one arm of the circuit breaker. This arrangement assures that the cooling fan will continue to operate in the event overheating should occur.

The output of one arm of relay 1 (compressor arm) is sent to the compressor regulator in the sensor electronics of the system support board and to the MJ4032 power transistor located above the power supplies. This power line (nominally +30 V) is isolated from the power for the rest of the electronics except at the interface box where they are tied together. The other arm of relay 1 (electronics arm) powers the coil of a switch closure relay (relay 3) and the coil and the input arms of relay 2. Relay 2 is used to stagger the inrush currents of the cooler compressor and the power supplies. The time delay between powering the compressor and then the electronics is provided by connecting the Logitek time delay unit to relay 2. The time delay, about 1.3 s, is set by an external resistor across terminals 1 and 4 of the time delay unit. The inputs and outputs of both arms of relay 2 are tied together to decrease overall contact resistance. The relay output is sent to the +5 and $\pm$15-V power supplies and to a low-power +20-V regulator located on the CCD bias board. The current capability of the +5-V supply is 5 A, and for the $\pm$15-V supply, $\pm$1 A. The +15-V power supply output is sent to the LM140K-12 +12-V regulator, also capable of a 1-A output current. Likewise, the –15-V output is sent to an LM120K-12, –12-V regulator, also capable of a 1-A output current.

The second thermostat is located at the input to the inverter of the cooling fan (BATAC) and serves to cut off the fan should the temperature in the sensor unit drop below 4°C, which may occur when the unit is first started in cold weather. The fan will remain off until the temperature exceeds 10°C.

The switch closure function is provided by relay 3 which is located under the rear bracket above the compressor. The relay coil is powered by the +30 V from the electronics output of relay 1, but is controlled by the computer using a transistor switch located on the system support board. The input and output of one arm of relay 3 is sent through the RFI/EMI enclosure via Erie filters and out the Bendix connector, through the data/power cable to the interface box.

The remaining signals passing through the RFI/EMI enclosure are Trans Data, Rec'd Data, Clr-to-send (these signals pass through Erie filters and OSM connectors and are communication lines between the computer in the sensor unit and the ground-based computer terminal), ϕ sync, CCD video signal (these pass through OSM connectors and are available at the interface box), and master reset, which comes from the interface box, through the RFI/EMI enclosure via an Erie filter to the computer and is used for resetting the computer.

B. INTERFACE BOX

A ground-based interface box is provided for connecting the sensor unit to the video terminal. The interface box also connects to the main dc power supply (nominally 32-V dc*) and houses two alarm devices (an acoustic alarm and a lamp) for intruder alert.

The interface box (BUD CU-1099HG, see Fig. 5) contains four connectors: a Bendix JT07-RE-20-16S(104), J_{1C}, an ITT Cannon DB25S, J_{4C}, and two Amphenol 31-238 BNC receptacles — J_2 and J_3. The Bendix connector, a 16-contact socket, connects to the data/power cable, a 150-ft cable that runs to the sensor unit. The ITT Cannon connector, a 25-contact socket, connects the video terminal (a Lear Siegler ADM-42) to the sensor unit. The BNC receptacles provide access to the sampled-and-held CCD output and to the ϕ_{sync} signal. Both BNC connectors are isolated from the chassis of the interface box by fiber glass inserts to minimize noise pickup on the outputs arising from the noisy chassis ground. The coax shield of the CCD output line serves as the ground for both the CCD video and ϕ sync.

Four switches are provided on the interface box. An Arrow Hart 35058, 20-A switch is used for system power ON/OFF. A momentary action switch, S4 (Dialight 571-1521-0101-011) is used for master reset. This switch resets the computer, which is required after every power-on. Two Dialight 571-1121-0101-011 switches (S_2 and S_3) are used as enable switches for a Dialco 812-1030-09-506 pilot lamp and a Mallary Sonalert SC648AH audible alert. If visual and/or audible alert is not desired, they can be switched off.

An 8-A ceramic "slo-blo" fuse is supplied for system protection against the 32-V main power supply. Four Smith 257 binding posts (two red, two black) are located inside the box. One set (BP1, BP2) is used to secure the incoming 32-V main power supply leads. The second set (BP3, BP4) is connected to the switch closure leads from the pole-mounted sensor unit. If an external alert is required, the wires presently on BP3 and BP4 can be disconnected and leads can be brought in through a small opening on the side of the box and connected to BP3 and BP4.

C. DATA/POWER INTERCONNECT CABLE

A power/data interconnect cable is required to connect the ground-based portion of the ADM to the pole-mounted sensor unit. Specifications of the cable are:

- 5, 20 AWG (19/30TC) conductors

- 9, 16 AWG (19/29TC) conductors per MIL-C-13777 compound "F")

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* The main power supply is adjusted to obtain 30 V at the input to the sensor unit (the electronics arm of the circuit breaker with the cooler compressor off). The main power supply voltage is about 32 V when the 150-ft data/power cable is used.

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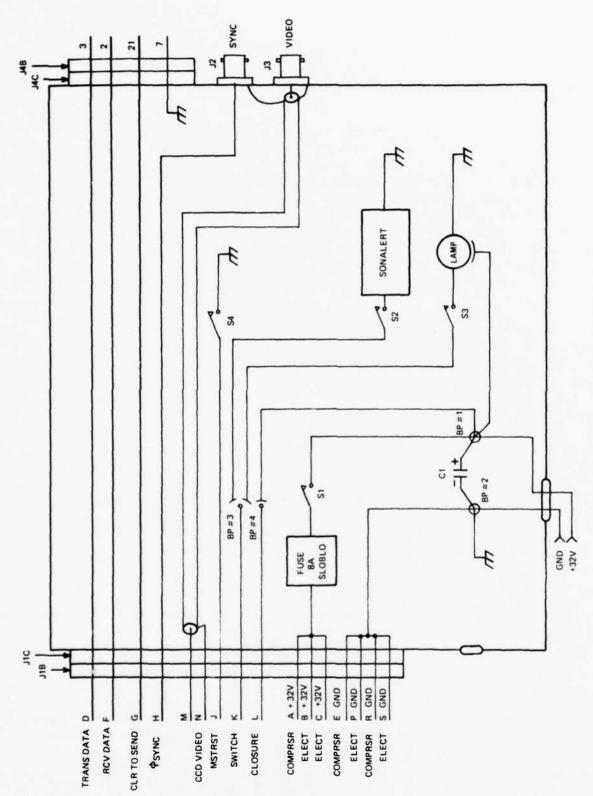
Fig. 5. Wiring arrangement of interface box.

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- 1, RG187A/U coaxial cable

- 1, overall shield, braided TC 34AWG with 90% minimum coverage

- 1, mylar binder - separator per MIL-1-C31, 0.001 x 1.00 under—over shield with 50% overlap

- Neoprene sheath, 0.090-inch wall thickness, single layer per MIL-C-13777

- Finished O.D. - 0.560-inch nom.

- Length of cable - 150 ft.

The cable provides wires for the following functions:
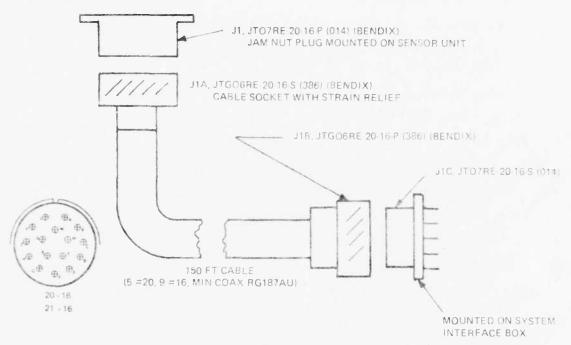
- 3, 16 AWG conductors for +32 V (drops to 30 V at input to sensor unit)

- 4, 16 AWG conductors for ground return

- 2, 16 AWG conductors for switch closure

- Terminal/Computer Lines

  - 1, 20 AWG conductor for "Transmit Data"

  - 1, 20 AWG conductor for "Rec'd Data"

  - 1, 20 AWG conductor for "Clr-to-Send"

  - 1, 20 AWG conductor for MSTRST (provided for resetting pole-mounted unit from ground)

  - 1, 20 AWG conductor for ϕ_{sync} (used for triggering ground-based ocsilloscope)

  - 1, RG187A/U coaxial cable for CCD CDS signal.

The sensor unit end of the cable is terminated with a Bendix connector, JTG06RE-20-16-S(386) and the interface box end with a Bendix JTG06RE-20-16-P(386). See Fig. 6.

D. EPROM EXPANSION BOARD

An EPROM expansion board will be used in ADMs 2 to 5 to implement the required parameter change algorithms and system diagnostic routines. Memory space is also required for future system software expansion.
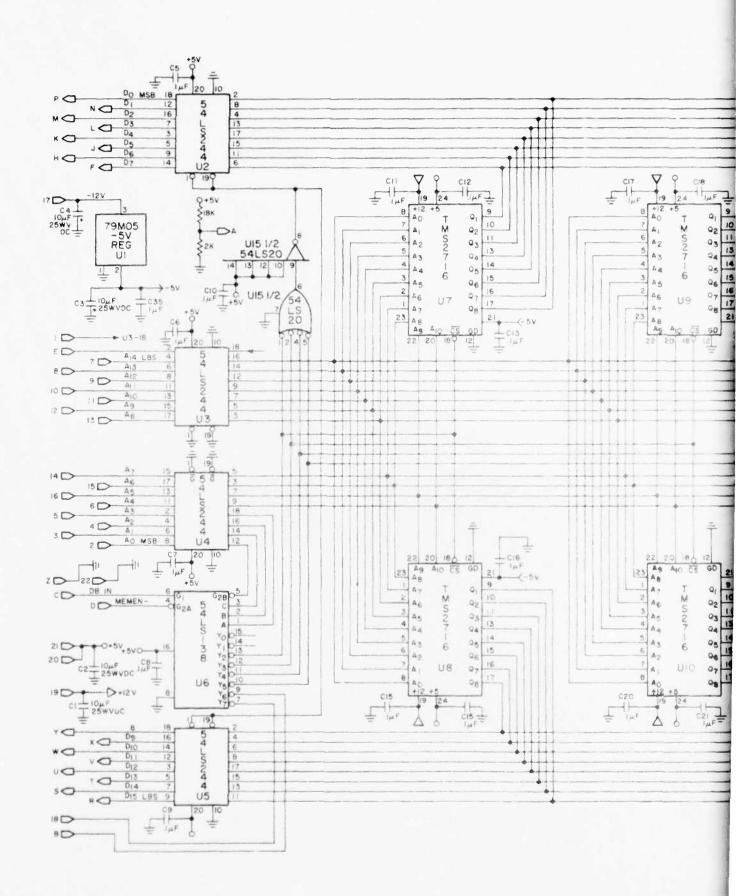
The EPROM expansion board (see Fig. 7) consists of eight TMS2716 2Kx8-bit EPROMs; four 54LS244 tristate buffers; a 54LS138 demultiplexer, and a 79MO5, -5-V regulator. The EPROMs are arranged in 8Kx16-bit words, and have access times of 450 ns. Each TMS2716 is specified to dissipate about 1-W under normal operating conditions. Its voltage requirements are +5 V, -5 V and +12 V. The -5 V is derived from the -12-V input using the 79M05. The tristate buffers

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J1, JTO7RE-20-16-P (014) (BENDIX)
JAM NUT PLUG MOUNTED ON SENSOR UNIT

J1A, JTGO6RE-20-16-S (386) (BENDIX)
CABLE SOCKET WITH STRAIN RELIEF

J1B, JTGO6RE-20-16-P (386) (BENDIX)

J1C, JTO7RE-20-16-S (014)

20 - 16
21 - 16

150 FT CABLE
(5 #20, 9 #16, MIN COAX RG187AU)

MOUNTED ON SYSTEM
INTERFACE BOX

CONNECTORS BENDIX JT (JUNIOR TRILOCK) - RE (ENVIRONMENTAL)
20 (SHELL SIZE, 20/16 IN.), 16 #16 CONTACTS

CONTACT	FUNCTION	WIRE SIZE & COLOR	COMMENTS
A	+32 V (COMPRESSOR)	#16 RED	
B	+32 V (ELECTRONICS)	#16 RED	
C	+32V (ELECTRONICS	#16 RED	
D	TRANS DATA	#20 WHT	DATA FROM TM990/101M TO TERMINAL
E	GND, COMPRESSOR	#16 BLK	
F	RCV DATA	#20 WHT	DATA FROM TERMINAL TO TM990/101M
G	COMPUTER CLR TO SEND	#20 WHT	FROM TM990/101M TO TERMINAL
H	0 SYNC	#20 WHT	
J	MASTER RESET	#20 WHT	FROM TERMINAL TO COMPUTER
K	SWITCH CLOSURE	#16 WHT	
L	SWITCH CLOSURE	#16 WHT	
M	CCD VIDEO CENT. COND COAX		OUTPUT OF ANALOG SIG COND BD
N	COAX SHLD, CCD VIDEO		
P	GND, ELECTRONICS	#16 BLK	
R	GND, COMPRESSOR	#16 BLK	
S	GND, ELECTRONICS	#16 BLK	

Fig. 6.   ADM data/power system interconnect cable.

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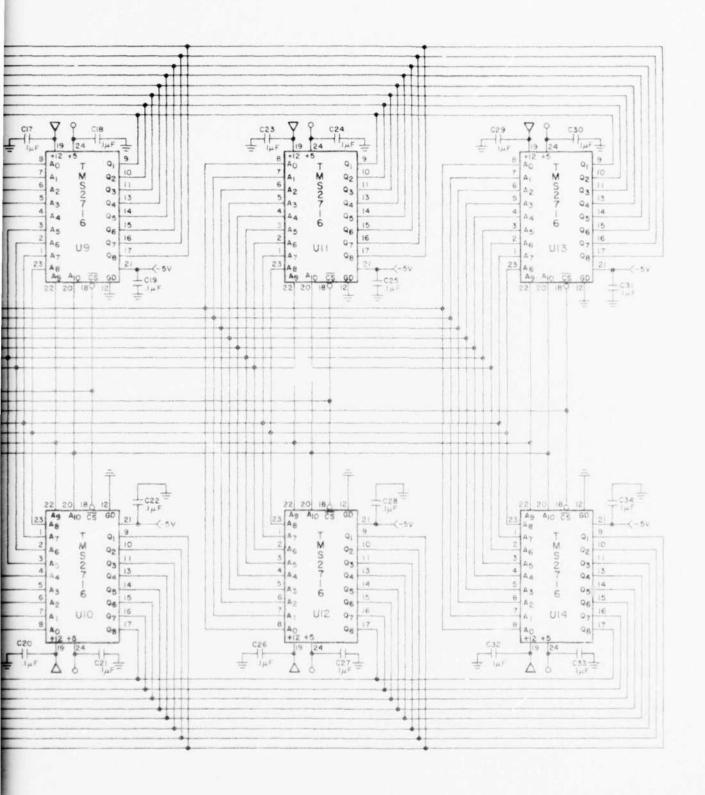
Fig. 7. EPROM expansion board schematic.

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isolate the data lines and address lines from their respective bus lines. Because the EPROMs are 8 bits in length, two EPROMs are required to form a 16-bit word. The demultiplexer decodes the most significant hex digit (MSHD) of the address line. The EPROM board address space is located from 2000 to 5FFF. Therefore, if the MSHD is decoded into a 2, 3, 4, or 5, the EPROM board is addressed. The least significant address bit (A15) is not decoded, hence only even addresses are used (i.e. 2000, 2002, etc.). The address designations on the EPROM board are listed in Table 1.

The EPROM board contains a two-resistor voltage divider from which the +5-V supply is divided and then multiplexed into the A/D. In this manner, the +5-V power supply can be monitored by the computer.

The need for the EPROM board developed after the system power design had been finalized and the power supplies had been ordered and received and after the heat dissipation considerations in the sensor unit had been finalized. With regard to the adequacy of the selected power supplies the added current requirements for the EPROM board are: 100 mA on the -15 V, 200 mA on the +15 V, and 1.2 A on the +5-V power supplies. The maximum output current of the $\pm$ 15-V power supply is $\pm$1 A and 5 A for the +5-V power supply. By referring to the power flow diagram in Fig. 8, it is seen that without the EPROM board the current draw is 375 mA on the +15-V supply, 225 mA on the -15-V supply, and 2.75 A on the +5-V supply. The total current values which will result when the EPROM board is included are enclosed in parentheses in Fig. 8. It is evident that the power supplies can accommodate the increased current requirements of the EPROM board.

Regarding adequacy of the present sensor unit cooling design, the EPROM board will, by itself, dissipate an additional 9 W and additional power dissipation will occur in power conditioning. The power dissipation of the supplies versus their output currents is shown in Figs. 9 and 10. Because of their increased efficiency with increased current load, the power dissipation does not increase linearly. The power dissipation in the +5-V supply only increases about 6 W and for the $\pm$15-V power supply about 4.5 W. Thus, the total increase in power dissipation resulting from the

TABLE 1. EPROM EXPANSION BOARD ADDRESS DESIGNATIONS

Address	EPROMs
2000 - 2FFF	U7, U8
3000 - 3FFF	U9, U10
4000 - 4FFF	U11, U12
5000 - 5FFF	U13, U14
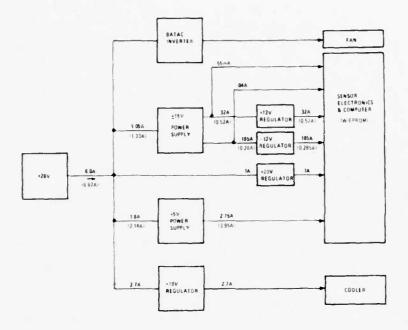
Fig. 8. Modified power flow diagram (parentheses enclose values of current with EPROM expansion board).
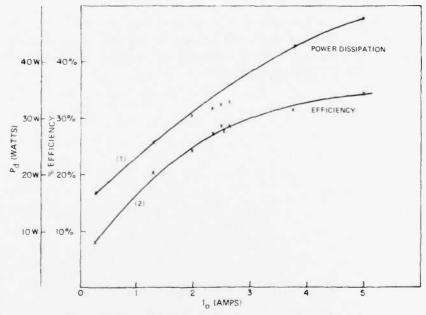
Fig. 9. Power dissipation vs. output current (I_O) of Abbott Transistor Labs Model SD 5.0 power supply (5-V dc, 5-A supply).

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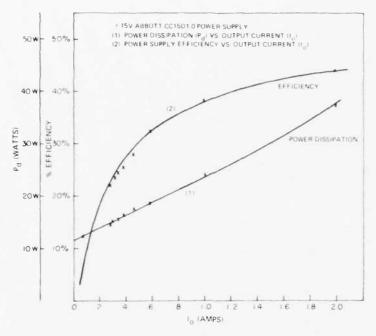
Fig. 10.   Power dissipation vs. output current (I_O) of Abbott Transistor Labs Model CC15D1.0 power supply (± 15-V, 1.0 A each output).

EPROM board is about 20 W and results in a 12 percent increase in total power dissipation in the sensor unit. It is not known at this time whether the cooling presently provided will be adequate and the extent of the changes required in the cooling design, if any, remain to be determined.

Section III

SYSTEM CHECKOUT AND OPERATION

With the exception of a few brief periods during which the CCD in the ADM-1B dewar (TC1258-1-B-3-23) could be cooled to a temperature low enough to operate the CCD at maximum integration, all system checkout has been performed using the output of an electrically inputted CCD operated at room temperature. In the electrically inputted CCD arrangement, the pulse applied to the electrical input of the CCD A-register can be made to vary in duration to generate rectangular outputs ranging from one to ten or more pixels wide to simulate targets such as persons and vehicles against a uniform background. In addition, the pulse amplitude can be varied to simulate targets having large or small temperature difference/emissivity products. The approach also permits one to vary the level of the uniform background throughout the full 5-V range of the A/D converter (by adjusting the clamp level in the analog signal conditioning circuit).

The simulation of an IR-responsive CCD with an electrically inputted CCD was first used in the Laboratory System, an arrangement used to check out the hand-wired prototypes of the ADM printed circuit boards and to examine the early computer EPROM sets. Following assembly and wiring of the ADM-1 sensor unit, checkout of the unit was begun using the output of an electrically inputted CCD.

Although the use of an electrically inputted CCD was necessitated by the lack of IR detection quality CCDs and by the lack of a dewar in which to cool the CCD, it proved to be very useful in checking out the bulk of the system and even in evaluating methods to reduce both computer- and cooler compressor-induced noise. (When evaluating cooler compressor induced noise, the CCD was connected to the ADM-1 sensor unit and the compressor was operated in ADM-1 with the cooler cold finger extending into air alone.)

Besides the limitation of not being able to exercise the chip temperature function of the system support board, operation in the CCD electrical inputting mode does not permit exercising the ALC (stare time control) function. With CCD electrical inputting, however, it is possible to check operation at either maximum or minimum integration (which is one-eighth of maximum integration). Operation at maximum integration is realized by starting up the system with the simulated background level at less than 1.5 V above ground. Once started, the simulated background can be lowered (to zero volts for example) or raised to a maximum of 4 V, the upper limit (for all but the minimum integration step) at which the system would switch to the next lower integration step when operating with an IRCCD-generated thermal background. With the simulated background, however, the system switches only between maximum and minimum integration. Operation at maximum integration can also be realized by starting up at minimum integration and then decreasing the simulated background to below

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1.5 V, the lower limit (for all but the maximum integration step) at which the system would switch to the next higher integration step when operating with an IRCCD.

Using the electrically inputted CCD approach to simulate targets and a uniform background has permitted checkout of the following in the ADM-1 system:

- The timing and control circuitry
- The CCD bias and driver circuitry
- The analog signal conditioning circuitry
- The analog-to-digital converter and associated digital gain
- Most of the system support board functions
- The power conditioning and control circuitry
- The RAM memory expansion board.

In addition, operation of the computer, interface box and video terminal was also established using the electrically inputted CCD approach. The approach was also used to check out the computer EPROM sets required to implement the modified Purdue algorithms planned for the ADM-1 system. Of the various EPROM sets, EPROM set 6 is the most complete set developed to date. The executive routine and the various subroutines and modules stored in EPROM set 6 (input load, spatial average, lossy integral, absolute value, decision module, classifier, etc.) are described in the Second Interim Report. Modifications in EPROM set 6 are required in the decision threshold module to take into account the automatic gain control factors of 1, 2, 4, and 8 when the integration period is max, and $1/2$, $1/4$, and $1/8$ of max, respectively as described in Section VII of this report.

A. SYSTEM NOISE

A noisy input into the A/D converter will cause bit flicker at the output of the converter which can be compensated by increasing the decision threshold increment (to avoid noise-generated false alarms) but at the expense of reduced system sensitivity.

1. CCD Pixel Fluctuation Noise

A major noise component was found to be the CCD pixel fluctuation noise which is evident at the output of the CCD. At room temperature and with the IR detectors biased off, the pixel fluctuation noise is typically 2 to 4 mV peak-to-peak and random in its occurrence, but a low frequency. It is much larger in amplitude than the higher frequency CCD noise components contained within each pixel. The CCD pixel fluctuation noise is believed to be associated with the CCD onchip output amplifier. In regards to the CCD pixel fluctuation noise,

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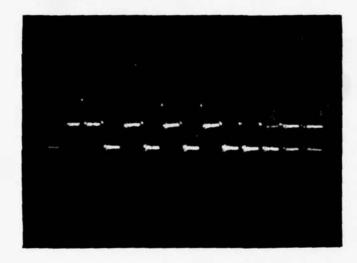
the only effect produced by the analog signal conditioning circuitry has been to amplify the pixel fluctuations by the voltage gain of the analog signal conditioning board. Unless a redesign of the onchip output amplifier or possibly different processing procedures occurs, it is believed that no further reduction in the CCD pixel fluctuation noise will be possible.

Other noise components that have appeared and that have been addressed during the development of ADM-1 include computer-induced noise and cooler compressor-induced noise. Both computer- and compressor-induced noise fall into the category of pickup type noise and are influenced by such factors as type of power conditioning power sharing, signal and supply line routing, shielding, and layout. In the ADMs, all power is provided by a common shelter-enclosed dc power supply. The power is then conditioned in the sensor unit to operate the CCD, the electronics, the computer, the cooler compressor and the inverter to power the cooling fan. The sharing of a common power source coupled with the close proximity of the subassemblies within the sensor unit is very conducive to pickup noise.

2. Computer-Induced Noise

Tests performed using the laboratory system and an electrically inputted CCD showed that the analog signal conditioning board was susceptible to computer-generated noise conveyed on lines from the computer that run to the RAM expansion board and then to the A/D board. This noise component, which was only evident when the computer was operating, caused the output pixels to ride on a large amplitude disturbance (35 mV peak-to-peak at the input to the A/D following a voltage gain of two) which was periodic at a frequency of about 1.8 kHz. Most of the computer-induced noise appeared to be associated with the 16 data lines and two control and two address lines which are all on a common computer board connector. It was found that when a metal shielding plate of the same size as the printed circuit boards was inserted between the A/D board and the analog signal conditioning board, the amplitude of the computer-induced noise was reduced to 20 to 25 mV peak-to-peak. For reference, when the computer was not operating (computer held at reset), the pixel fluctuations were due entirely to CCD pixel fluctuation noise (4 to 6 mV peak-to-peak at the input to the A/D converter) which is not periodic. The 4-to-6 mV pixel fluctuations into the A/D converter resulted in flicker at the output in only the three least significant bits (see Fig. 11).

To minimize the computer-generated noise in the ADMs, the analog signal conditioning board is separated from the A/D board by four nondigital boards and sandwiched between a shield plate (over its top side) and the base plate of the ADM, so that both surfaces of the analog signal conditioning board face gounded shield plates. In this arrangement, the resulting pixel flucutation noise is nearly the same whether the computer is operating or not as may be seen from the two oscilliscope traces of Fig. 12.

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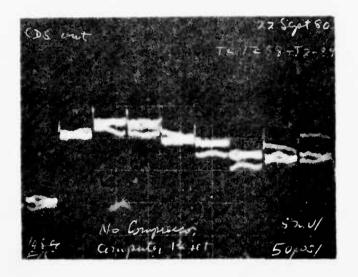
- SERIAL OUTPUT OF A/D
  CONVERTER SUMMED WITH CLOCK
  5 V/div
  1 μ s/div
- FLICKER IS PRESENT IN ONLY THE
  2^0, 2^1 AND 2^2 BITS
- PIXEL FLUCTUATION NOISE
  AT INPUT, 4 TO 6 mV/pp
- OUTPUT OF A/D INVERTED – TO
  BE READ AS STRAIGHT BINARY
- CCD OPERATING AT ROOM TEMP.
- LABORATORY SYSTEM
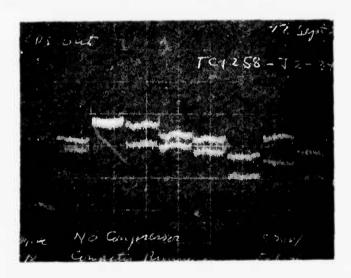
Fig. 11. Serial output of A/D eonverter with computer held at reset.

3. Cooler Compressor-Induced Noise

Noise at the input to the A/D, generated when the cooler compressor was operating with the original power wiring arrangement, was found to be about 30 mV peak-to-peak. In the original arrangement, a common ground and a common input line (30-V dc at the input to the sensor unit) supplied power to dc-to-dc power supplies required to operate the clectronics and the eomputer and also supplied the input power to the power regulator (+19-V output) used to operate the eooler compressor. The compressor-induced noisc at the input to the A/D converter (following a 2X gain in the analog signal conditioning circuit) is shown in Fig. 13 for which separate input lines were used; the ground return lincs were common. In this case, the CCD (TC1258-J2-34) was operating at room temperature and was plugged into the socket that would normally connect ADM-1 to a CCD in the dewar. (An operating CCD in a dewar was not available.) The noise ean be seen to consist of a low frcquency and a higher frequency eomponent. The low frequency component is large in amplitude and its frequency of 25 Hz corresponds to the 1500-RPM cycle rate of the cooler. The higher frequeney component, which is usually less than 10 mV peak-to-peak oecurs at a frequency of 300 Hz and eorresponds to the pole switching rate of the brushless dc motor.

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A. COMPUTER OPERATING
5 mV/div
50 μs/div

B. COMPUTER NOT OPERATING
(HELD AT RESET)
5 mV/div
50 μs/div

• ROOM TEMPERATURE OPERATION
• IR DETECTORS BIASED OFF
• IRCCD TC1258-J2-34

Fig. 12. Pixel fluctuation noise with computer operating and not operating at the input to the A/D converter of ADM-1 (the CCD pixel fluctuation noise is one-half of the above).

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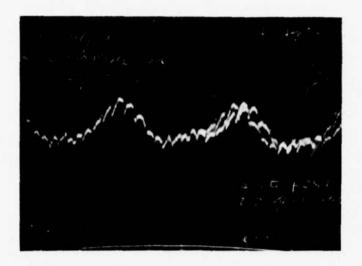
Fig. 13. Cooler compressor-induced noise at the input to the A/D converter prior to separating the input power lines in the ADM-1 sensor unit.

To eliminate the cooler compressor-induced noise, it was necessary to run both a separate input power line and a separate return line to the compressor power regulator. The need to provide separate lines to power the cooler compressor required reapportioning the power lines within the signal/power interconnect cable. The resulting pixel fluctuation noise at the input to the A/D converter (following a 2X gain) after separating the input power and return lines to the compressor power regulator is shown in Fig. 14. The peak-to-peak pixel fluctuations are seen to be less than 5 mV.

B. MINIMUM DECISION THRESHOLD INCREMENT

The results of a system checkout trial using an electrically inputted CCD (CCD TC1258-J-2-34) to determine the minimum decision threshold increment for which the system could detect a two-pixel wide target without generating false alarms are shown in Table 2. In this checkout trial, the simulated background was varied from 1000 mV to 4000 mV and the hexadecimal value of the computer-stored threshold count associated with each background level was called up from the computer and displayed on the video monitor. In all cases, the amplitude of the two-pixel wide target was 20 mV greater than the background. The target was detected, and its location and size were properly displayed on the video monitor at each of the background levels. False alarms (as observed over a 20-minute period) occurred only for threshold counts less than 0008. These results indicate that the ADM-1 system noise limits the minimum decision threshold increment to a hex count value of 0008, corresponding to 9.768 mV.

5 mV/div
50 μs/div

Fig. 14. Pixel fluctuation noise at the A/D input (A_V=2) following separation of power
input and return lines to the compressor power regulator.

C. VOLTAGE ON SKIMMING BARRIER GATE

The voltage applied to G_{1T}, the skimming barrier gate which maintains a contin-
uous reverse bias on the Schottky barrier diodes (also called the first parallel transfer
gate) affects both the resulting dark current level and the sensitivity of the Schottky
detectors. If the CCD is not cooled to a sufficiently low temperature, the detector
dark leakage current can be large enough to result in a saturated output even at rela-
tively low values of V_{G1T}. The variation in dark level plus IR-induced background with
V_{G1T} at 25 percent integration (27.32 ms) and at a chip temperature estimated to be
83°K is shown in Fig. 15. The measurements were made following cooldown run
2-18-11-802 (ADM-1B dewar containing CCD TC1258-1-B-3-23). The detector array
was viewing a uniform room temperature background (a laboratory wall) estimated to
be at 295°K. The voltages applied to the CCD during the measurements are listed
in Table 3.

From Fig. 15, it is seen that at V_{G1T} 0 V, the detector output is about 30 per-
cent of the saturation level (saturation at the input to the A/D converter was 3.35 V
with the analog signal conditioning voltage gain at two) and rises rapidly with increasing
V_{G1T}. At V_{G1T} = 2.0 V (the channel threshold voltage under gate G_{1T} at 77°K is about
2 V, Kosonocky et al.[2]), the resulting output is withing 75 percent of saturation
leaving only 25 percent useful dynamic range. The data of Fig. 15 indicate that the
CCD when operating at the estimated chip temperature of 83°K is not cold enough to
operate well even at the 25 percent integration step.

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TABLE 2. DECISION THRESHOLD VS. ELECTRICALLY INPUTTED BACKGROUND
AND OCCURRENCE OF FALSE ALARMS

Electrically Inputted Background V_B (mV)	Threshold Increment Count (Hex)	Threshold Increment, V_d (mV)	False Alarms
1000	0007	8.547	Yes
1250	0008	9.768	No
1500	0008	9.768	No
2000	000A	12.21	No
3000	000B	13.43	No
4000	000D	15.87	No

Conditions

- ADM-1

- EPROM set 6

- Maximum integration

- Two-pixel wide target at sensors 36 and 37

- Cooler compressor running

- 150-ft data/power cable

- Minimum detected target — 20 mV

- False alarm observation period - 20 min

- CCD TC1258-J-2-34 at room temperature
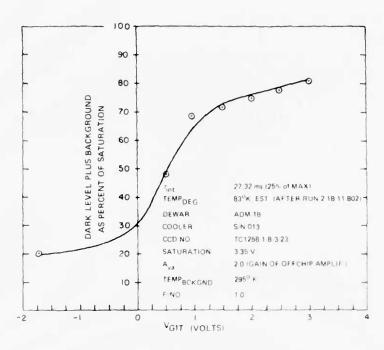
Fig. 15. Dark level plus background vs. V_{G1T} at 25% integration.

A second plot of dark level plus background versus V_{G1T} but at 50 percent integration (54.64 ms) is shown in Fig. 16. Except for the integration duration, the conditions are identical to Fig. 15. From Fig. 16, it is seen that at $V_{G1T} = 0$ V the combined dark level plus background of the array exceeds 60 percent of the saturation level. At the highest V_{G1T} shown, 0.375 V, the combined dark level and background exceeds 85 percent of saturation showing again that chip temperature is not low enough.

The variation of signal output with V_{G1T} at 25 percent integration is shown in Fig. 17 for which the conditions are identical to Fig. 15. Here, the target was a human hand which was inserted into the field of view of the detector array while the array was viewing a uniform laboratory background at an estimated temperature of 295°K. The target is estimated to be 15°K warmer than the background. The maximum signal produced by the target was about 300 mV which corresponds to a maximum sensitivity of about 730 mV/($^{\circ}$K-s) at the input to the A/D or 365 mV/($^{\circ}$K-s) at the output of the CCD. At $V_{G1T} = 0$ V, the signal is 65 percent of the maximum which is attained at about $V_{G1T} = 2.0$ V.

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TABLE 3. VOLTAGES APPLIED TO CCD (TC1258-1-B-3-23) DURING MEASUREMENTS OF V_{G1T}

FUNCTION	VOLTAGE (V)
V_{STR}	-3.66
V_{TFR}	-11.97
D1	18.75
DS1	16.27
DS2	gnd
V_R	8.20
V_{G1T}	varied
V_{G2T}	10.0
V_{G3T}	9.77
V_{G4T}	6.00
G4	3.47
G1	-6.51
V_{G2A}	0.50
V_{G2B}	-12.0
V_{S1}	12.87
V_{int}	2.70
V_{CLK}	9.50

DARK LEVEL PLUS BACKGROUND
AS PERCENT OF SATURATION

100
90
80
70
60
50
40
30
20
10

τ_{int} 54 64 MS (50% OF MAX)
$TEMP_{DET}$ 83°K, EST (AFTER RUN 2 18 11 802)
DEWAR   ADM 1B
COOLER   S/N 013
CCD NO   TC1258 1 B 3 23
SATURATION   3 35 V
A_{va} 2 0 (GAIN OF OFFCHIP AMPLIF)
$TEMP_{BCKGND}$ 295°K
F/NO   1 0

-3   -2   -1   0   .1   .2   .3   .4

V_{G1T} (VOLTS)
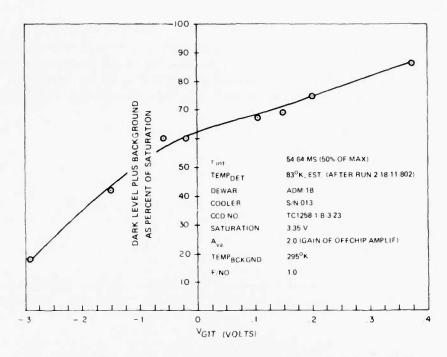
Fig. 16. Dark level plus background vs. V_{G1T} at 50% integration.

RELATIVE SIGNAL

1.0
.9
.8
.7
.6
.5
.4

τ_{int} 27.32 ms (25% OF MAX)
$TEMP_{DET}$ 83°K EST (AFTER RUN 2-11-11-802)
DEWAR   ADM-1B
COOLER   S/N 013
CCD NO.   TC 1258-1-B-3-23
MAX SIGNAL   300 mV
TARGET-BCKGND $\triangle T$ 15°K (EST)
A_{va} 2.0 (GAIN OF OFFCHIP AMPLIF)
$TEMP_{BCKGND}$ 295°K
F/NO   1.0
(TARGET IS HUMAN HAND)

-2   -1   0   1   2   3   4

V_{G1T} (VOLTS)
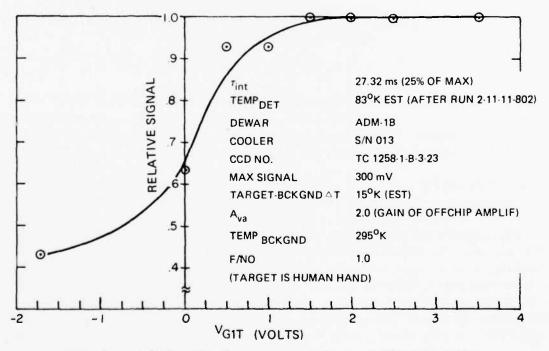
Fig. 17. Relative signal response vs. V_{G1T} at 25% integration.

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Although the sensitivity value of 365 mV/($^{\circ}$K-s), which is normalized to unity F/No, is an approximate value, it is of interest to compare it to another sensitivity value. Such a sensitivity value may be determined from measurements made at RADC/ET using a thick platinum silicide IRCCD by R.W. Taylor of RADC/ET and reported by Kosonocky et al.[2] The data given in this reference are:

- T_{bckgnd} = 300°K
- T_{TRGT} = 23°K (50°C slit)
- τ_{int} = 35 ms
- Lens F/No = 1.2
- V_{G1T} = 4.16 V
- T_{array} = 80°K.
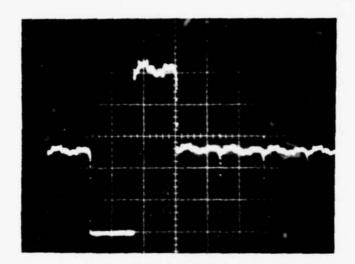
The resulting background plus dark level was 300 mV and the signal produced by the 23°K temperature difference was 108 mV. Using the above data, the sensitivity which is given by

$$\text{Sensitivity} \atop (\text{F/No=1}) = \frac{V_{sig}\,(\text{F/No})^2}{\tau_{int}\,\Delta T}$$

$$= (108\text{ mV})\,(1.2)^2 / \,(35\text{ ms x }23^{\circ}\text{K})$$

$$= (193\text{ mV/ }(^{\circ}\text{K-s})$$

The two sensitivities differ by a factor of 1.9 which may, in part, reflect the improved sensitivity of thin platinum silicide IRCCDs over their earlier thick platinum silicide counterparts. Other differences in the two setups such as lens and filter transmission, which are not taken into account here, would alter the results.

D. OPERATION OF ARRAY IN ADM-1 AT THE 12.5, 25, and 50 PERCENT INTEGRATION STEPS

The output of the IRCCD array in the ADM-1B dewar when cooled to an estimated 83°K and when viewing the laboratory background is shown in Fig. 18 with the array operating at the 12.5 percent integration step (the minimum integration step, equal to 13.66 ms) and in Figs. 19 and 20, with the array operating at the 25 percent and at the 50 percent integration steps, respectively. The relationships between the valid video output, the dumped outputs, are illustrated in each of the figures. The valid video output is acted upon by the A/D converter whose 256 start convert pulses
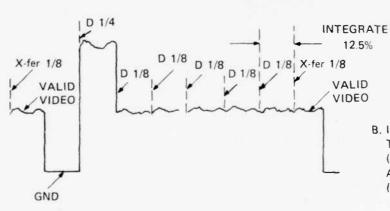
A. OPERATION AT 12.5% INTEGRATION
$V_{G1T} = + 3.0$ V

500 mV/div
10 ms/div

B. ILLUSTRATION OF VALID VIDEO
TRANSFER AT 12.5% INTEGRATION
(X-fer 1/8) AND ASSOCIATED 1/4
AND 1/8 INTEGRATION DUMPS
(D 1/4 AND D 1/8)

CCD NO. TC1258-1-B-3-23
DEWAR ADM-1B
COOLER S/N 013
CHIP TEMP. = 83°K (EST) FOLLOWING RUN 2-18-11-802
OFFCHIP VOLTAGE GAIN = 2.0
T_{BCKGND} = 295°K
F/NO = 1.0

Fig. 18. Operation of array at the 12.5% integration step (12.5% is minimum integration).

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A. OPERATION AT 25% INTEGRATION
   V_{GIT} = +0.50 V
   500 mV/div
   10 ms/div

X-fer 1/4   VALID   X-fer 1/4
VALID   D 1/4   VIDEO
VIDEO   D 1/8 D 1/8 D 1/8   D 1/8

B. ILLUSTRATION OF VALID VIDEO
   TRANSFER AT 25 % INTEGRATION
   (X-fer 1/4) AND ASSOCIATED 1/4
   AND 1/8 INTEGRATION DUMPS
   (D 1/4, D 1/8)

INTEGRATE
25%

GND

CCD NO. TC1258-1-8-3-23
DEWAR ADM-1B
COOLER S/N 013
CHIP TEMP. = $83^{o}K$ (EST) FOLLOWING RUN 2-18-11-802
SATURATION = 3.35 V (AT INPUT TO A/D)
OFFCHIP VOLTAGE GAIN = 2.0
T_{BCKGND} = $295^{o}K$ (EST)
F/NO = 1.0

Fig. 19.   Operation of array at the 25% integration step.

A. OPERATION AT 50% INTEGRATION

$V_{GIT} = + 0.057$ V

500 mV/div
10 ms/div

GND

B. ILLUSTRATION OF VALID VIDEO
TRANSFER AT 50% INTEGRATION
(X-fer 1/2) AND ASSOCIATED 1/4
AND 1/8 INTEGRATION DUMPS (D 1/4, D 1/8)

CCD NO. TC1258-1-B-3-23
DEWAR ADM-1B
COOLER S/N 013
CHIP TEMP. = 83°K (EST) FOLLOWING RUN 2-18-11-802
SATURATION = 3.35 V (AT INPUT TO A/D)
OFFCHIP VOLTAGE GAIN = 2.0
$T_{BCKGND} = 295$°K (EST)
F/NO = 1.0

Fig. 20. Operation of array at the 50% integration step.

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occur only during the valid video output period. Array readout occurs at the rate of 18,740 pixels/s (256 pixels in 13.66 ms). The waveforms in Figs. 18, 19, and 20 show the input to the A/D converter after the CCD output has been reference clamped to ground, sampled-and-held, and amplified by a factor of two in the analog signal conditioning circuitry. Selection of the integration steps was operator-controlled from the computer terminal. In this mode, the computer does not process the incoming data. The output of the array consists of the thermally generated dark current level plus the infrared-induced background. The temperature of the background, the laboratory wall, is estimated to be $295^\circ K$.

Figures 21, 22, and 23 show the valid video output of the array at an expanded time base, and the response of the array to a broad area target, a human hand, with the array operating at the 12.5, 25 and 50 percent integration steps, respectively. Figures 21, 22, and 23 show that detector sensitivity is not uniform across the array. The array is least sensitive at the start of output, corresponding in array location to the output end of the array, with sensitivity peaking between 6 and 12 ms of readout which corresponds to detectors located near the center and toward the electrical input end of the array. The increase in nonuniformity of the output with increasing integration time is apparent. It is also apparent that despite relatively low value of V_{G1T}, at 25 and 50 percent integration, the resulting dark level plus background is a high percentage of the array's saturation output. Both increased nonuniformity and large amplitude output at low values of V_{G1T} are indications of excessive dark current leakage.

The response of the array to a low-temperature background is shown in Fig. 24 in which the array is operating at 12.5 percent integration as in Fig. 18. The upper trace shows the dark current level and background resulting when the array is viewing a $295^\circ K$ background, while the lower trace shows the array output when the entire field of view is covered w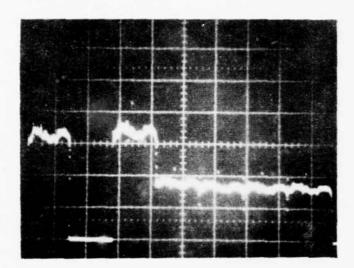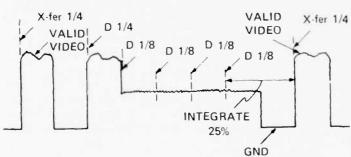ith a low-temperature background. The low-temperature background condition was achieved by covering the lens assembly with a styrofoam cup into which liquid nitrogen had been poured.

Although the temperature of the low-temperature background is not known, it is believed to be low enough to result in a negligible infrared-induced background. The bulk of the output when viewing the low-temperature background is therefore believed to be dark leakage current from the detector array.
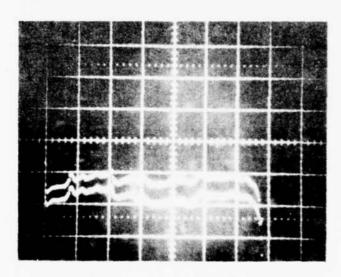
A. OUTPUT OF ARRAY AT 12.5%
INTEGRATION (13.66 ms)

$V_{GIT} = + 3.00$ V

500 mV/div

2 ms/div

DARK LEVEL PLUS BACKGROUND IS
ABOUT 1.3 V (0.39 OF SATURATION)

B. DOUBLE EXPOSURE SHOWING
RESPONSE AT 12.5% INTEGRATION
TO A HUMAN HAND

$V_{GIT} = + 3.00$ V

200 mV/div
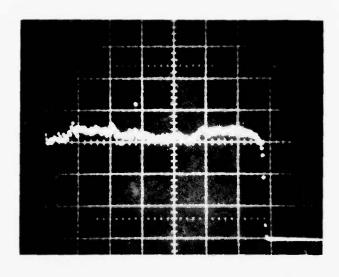
2 ms/div

RESULTING SIGNAL VARIES FROM
100 mV (AT START OF OUTPUT) TO
140 mV (BETWEEN 6 AND 12 ms)

$\text{MAX SENS} = \dfrac{340 \text{ mV}}{^\circ K - s}$ (AT CCD)

CCD NO. TC1258-1-B-3-23
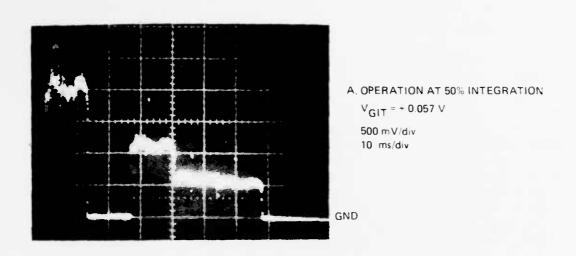DEWAR ADM-1B
CHIP TEMP. = 83° (EST) FOLLOWING RUN 2-18-11-802
SATURATION = 3.35 V AT INPUT TO A/D
OFFCHIP VOLTAGE GAIN = 2.0
$T_{BCKGND} = 295°K$ (EST)
F/NO = 1.0

Fig. 21. Output of IRCCD array when operating at the 12.5% integration step and
response to a broad area target.

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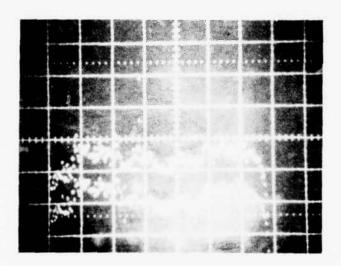
A. OUTPUT OF ARRAY AT 25% INTEGRATION (27.32 ms)

$V_{GIT} = + 0.50$ V

500 mV/div

2 ms/div

DARK LEVEL PLUS BACKGROUND IS BETWEEN 1.5 AND 1.7 V, (0.45 AND 0.51 OF SATURATION)

B. DOUBLE EXPOSURE SHOWING RESPONSE AT 25% INTEGRATION TO TO A HUMAN HAND

$V_{GIT} = + 0.50$ V
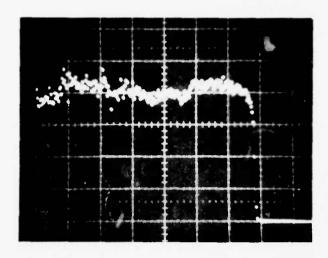
200 mV/div

2 ms/div

RESULTING SIGNAL VARIES FROM 200 (AT THE START OUTPUT) TO 280 mV (BETWEEN 6 AND 12 ms)

$$\text{MAX SENS} = \frac{340 \text{ mV}}{^{o}K - s} \quad \text{(AT CCD)}$$

CCD NO. TC1258-1-B-3-23
DEWAR ADM-1B
CHIP TEMP. = $83^{o}K$ (EST) FOLLOWING RUN 2-18-11-802
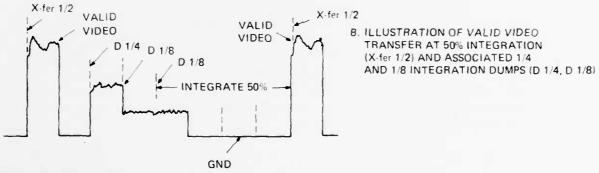SATURATION = 3.35 V (AT INPUT TO A/D)
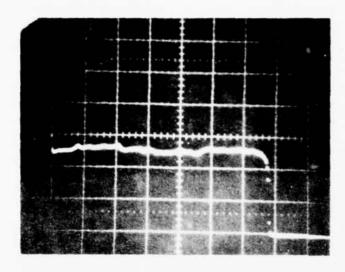OFFCHIP VOLTAGE GAIN = 2 0
$T_{BCKGND} = 295^{o}K$ (EST)
F/NO = 1.0

Fig. 22. Output of IRCCD array when operating at the 25% integration step and response to a broad area target.
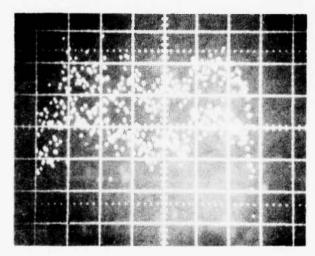
A. OUTPUT OF ARRAY AT 50%
   INTEGRATION (54.64 ms)

   V_{GIT} = +0.057 V

   500 mV/div
   2 ms/div

   DARK LEVEL PLUS BACKGROUND
   IS BETWEEN 1.8 AND 2.4 V,
   (0.54 AND 0.72 OF SATURATION)

B. DOUBLE EXPOSURE SHOWING
   RESPONSE OF ARRAY TO A
   HUMAN HAND

   V_{GIT} = +0.057 V

   200 mV/div
   2 ms/div

   RESULTING SIGNAL VARIES FROM
       220 mV (AT START OF ARRAY OUTPUT)
   TO
       330 mV (BETWEEN 6 AND 12 ms)
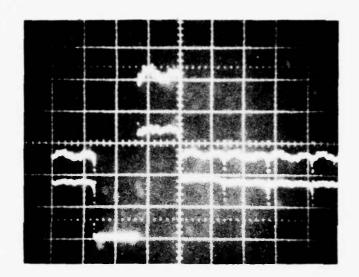
   $$MAX\ SENS = \frac{200\ mV}{^\circ K - s}\ (at\ CCD)$$

CCD NO. TC1258-1-B-3-23
DEWAR ADM-1B, COOLER S/N 013
CHIP TEMP. = $83^\circ K$ (EST) FOLLOWING RUN 2-18-11-802
SATURATION = 3.35 V AT INPUT TO A/D
OFFCHIP VOLTAGE GAIN = 2.0
T_{BCKGND} = $295^\circ K$ (EST)
F/NO = 1.0

Fig. 23.   Output of IRCCD array when operating at the 50% integration step and
response to a broad area target.

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A. ARRAY OPERATING AT 12.5%
INTEGRATION

$V_{GIT} = + 3.0$ V

500 mV/div

10 ms/div

UPPER WAVEFORM IS ARRAY
OUTPUT FOR 295°K BACKGROUND

LOWER WAVEFORM IS ARRAY
OUTPUT FOR A LOW TEMPERATURE
BACKGROUND PRODUCED BY
COVERING THE LENS ASSEMBLY
WITH A STYROFOAM CUP IN WHICH
LN_2 HAD BEEN CONTAINED

DETECTOR ARRAY OUTPUT (mV)

	AT 1/8 INT (13.66 ms)	AT 1/4 INT (27.32 ms)
DARK OUTPUT + 295°K BCKGND	1300 (39% SAT)	2600 (78% SAT)
DARK OUTPUT + LOW TEMP. BCKGND	850 (25.4% SAT)	1700 (50.8% SAT)

Fig. 24. Array output when viewing a 295°K and a low-temperature background.

Section IV
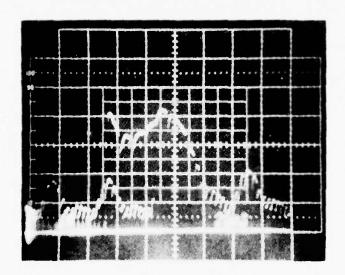
COOLERS

During the period covered by this interim report, the five one-watt, split-cycle coolers required for the program were received. The coolers are identified by the serial numbers S/N 009, S/N 011, S/N 012, S/N 013, and S/N 014.

A. STARTUP AND INRUSH CURRENT

It was found that a reliable startup of the coolers could not be realized at an 18-V input, and it was necessary to increase the input voltage. Startup has been reliable at 19 V. The inrush current of one of the coolers (S/N 012) was measured by monitoring the IR drop across a series-connected 0.05-ohm resistor. The peak of the inrush current was 8.4 A and the duration of the inrush was about 70 ms. The inrush current waveform as seen on a storage oscilloscope is shown in Fig. 25. The smaller amplitude waveforms to the left and right of the two inrush peaks depict the steady-state current drawn by the cooler compressor.

Each of the five coolers has been operated and a number of deficiencies have been noted.

2 A/div
20 ms/div

Fig. 25. Inrush current of a de-powered, one-watt, split-cycle cooler (cooler S/N 012, $V_{in} = 18$ V).

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B. COOLER S/N 009

Cooler S/N 009, which appeared to be operating well at one time, failed to oper-
ate during a startup test (1 October 1980) and was returned to the manufacturer. In
the failed condition, the cooler exhibited large input resistance and would only draw
30 mA at an 18-V input. It was reported that failure was due to the burnout of two thin
bonding wires, an input and an output wire to a hybrid chip. These wires carry power
and also serve as fuse links to protect the dc motor's switching circuitry. In the earlier
coolers, a single wire was used in these links, but because of the burning out of the
links, each single wire was replaced with a pair. It was reported by the manufacturer
that the remaining coolers each use paired fuse links.

C. COOLER S/N 011

This cooler experienced a sharp decrease in cooling capacity after operating well
for about 5-1/2 hours. The current drawn by the cooler, which had been 3.0 A at a
19-V input while cooling the CCD in the ADM-1B dewar, dropped to about 2 A after the
cooler was turned off for about three minutes and restarted. It appears that cooler S/N
011 may have experienced a "short-stroke" mode failure. In the short-stroke mode, the
displacer becomes constrained and does not undergo full travel; the cooler performs
less work and therefore also draws less current and is unable to cool a given load to
a lower temperature. It is our understanding that the buildup of contaminants or the
presence of small impurity particles can lead to the short-stroke condition. Cooler
S/N 011 was returned to the manufacturer to be examined and repaired.

D. COOLER S/N 013

This cooler experienced a decrease in its leveling-off current (the steady-state
current, reached typically about 18 minutes into a cooldown run) after nine cooldown
trials totaling about 10 hours of cooler operation. In the first cooldown run with cooler
S/N 013 (run 1-17-11-801), the leveling-off current was 2.80 A and was attained after
18 minutes of operation. In this run, the cooler was connected to the ADM-1B dewar,
a standard-height fuzz button was used in the thermal interface between the tip of the
cooler cold finger and the dewar top cap to which the CCD package is soldered, and the
cryopumped vacuum region (the region between the cooler cold finger and the inner sur-
face of the glass lead frame) was filled with air. In the ninth and final cooldown run
(run 5-21-11-802), under conditions identical to the first cooldown run, the leveling-
off current was 1.85 A corresponding to a decrease of almost 34 percent over the
leveling-off current measured during the first cooldown run. Because of the decreased
input current of cooler S/N 013, it has been returned to the manufacturer.

E. COOLER S/N 014

Cooling of the ADM-1B dewar to a temperature low enough to permit a positive
bias on G_{1T} was never attained with cooler S/N 014 (three cooldown runs). The
leveling-off current of cooler S/N 014 which was initially about 3.4 A decreased to

about 3.0 A. It is not known whether the cooler has degraded or whether the decrease in current reflects an increase in the thermal load (a cooler acting against a large thermal load will draw less current).

F. COOLER S/N 012

This cooler initially exhibited erratic current surges and an occasional clanging noise and because of this behavior, its condition was suspect. However, the cooler has been used in four cooldown runs, and it appears to be performing well. Typically cooler S/N 012 draws between 1.80 and 1.85 A at the start of cooldown and attains a leveling-off current of between 2.55 and 2.65 A, when inputted with 19 V.

Section V

COOLDOWN TRIALS

A number of attempts were made to cool the CCD in the ADM-1B dewar (TC1258-1-B-2-23, a thin platinum silicide device obtained from the Air Force on 8 August 1980) using coolers S/N 011, 012, 013, and 014. In all, 16 cooldown runs with the ADM-1B dewar were performed using various arrangements. The arrangements included use of a standard-height fuzz button, a reduced-height fuzz button and noncontacting gaps in the thermal interface between the cooler cold finger tip and the dewar top cap to which the CCD package is soldered. Also used were air, nitrogen, and acetone in air in the cryopumped dewar region. Except for a few brief periods, cooling of the CCD in the ADM-1B dewar to a temperature low enough to allow a positive bias to be applied to G_{IT} (the charge skimming barrier gate) could not be realized when operating at maximum integration (109.27 ms).

During the early cooldown attempts the CCD would reach an operating temperature within 10 to 20 minutes, while the voltage across the onchip temperature sense diode would pass through a maximum. By the end of the run, typically 30 minutes, the voltage would be significantly less than the peak value indicating the minimum temperature had been reached and that the chip was warming up. In subsequent cooldowns, the durations of the runs were increased to further examine what appeared to be a warmup effect. In these longer runs, it was found that the chip temperature under some conditions actually cycled through a series of minima and maxima.

The variation in chip temperature with time during the cooldown run (run 1-17-11-801) in which cooler S/N 013 was operated for the first time at RCA is shown in Fig. 26. The cooler cold finger tip-to-dewar top cap thermal interface consisted of a standard fuzz button (0.125 inches high and 0.560 inches in diameter), the input voltage to the cooler compressor was 19-Vdc, and air initially at a pressure of one atmosphere was contained in the cryopumped region of the dewar. (In two subsequent runs, dry nitrogen gas was used.)

The temperatures given in Fig. 26 and throughout this report are estimated values and may be favoring the low side. The onchip diode temperature calibration did not hold for the CCD in the ADM-1B dewar (reason not understood) and the temperatures given are corrected for the room temperature difference in the diode voltage ($50 \text{ mV} \div 2 \text{ mV/}^{O}\text{K} = 25^{O}\text{K}$) and an additional 15°K which represents the high side of the difference in the temperature sense diode voltages between the CCD operating and not operating. Thus, the temperatures given for the CCD of the ADM-1B dewar are less than the values obtained from the diode calibration data by 40°K.

As given in Fig. 26, the minimum temperature reached was 72°K and was obtained 18 minutes after turning on the cooler. The first maximum in the subsequent temperature cycling was about 91°K and was attained 28 minutes after cooler turnon. The
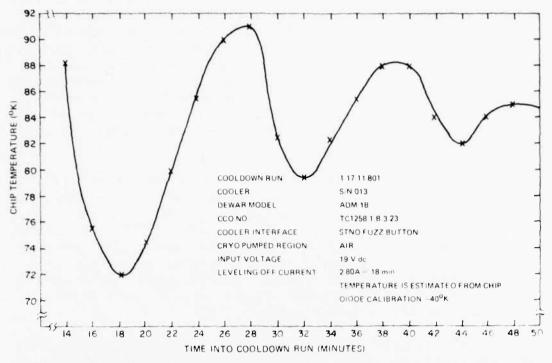
Fig. 26. Variation of chip temperature with cooldown time (run 1-17-11-801).

periodicity of the temperature cycling decreases with time and the amplitudes of the temperature excursions are seen to decrease progressively. The difference between the first minimum (at 18 minutes) and the first maximum (at 28 minutes) is about $19^{O}K$ while the difference between the third minimum (at 44 minutes) and the third maximum (at 48 minutes) is only $3^{O}K$. It appears that the temperature cycling will eventually damp out and that the temperature will then remain around $83^{O}K$.

The temperature cycling effect, although not fully understood, appears to be related to the repeated formation and boiling-off of liquefied gas. It is believed that liquefication and boiling-off of oxygen and nitrogen contained in the cryopumped dewar region affect both the thermal resistance of the interface between the cooler cold tip and the dewar top cap and convective heat transfer in the cryopumped dewar region.

Prior to turning on the cooler, the gas in the cryopumped region is at room temperature and at a pressure of one atmosphere. During cooldown, the temperature of the gas becomes reduced as does the gas pressure. At some point, some of the gas liquefies at the coldest region of the cold finger which is the top of the cold finger. The fuzz button is compressed between the top of the cold finger and the dewar top cap. The presence of liquefied gas within or along the periphery of the fuzz button improves thermal conduction to the dewar top cap and the decreased gas pressure leads to reduced heat transfer by convection in the cryopumped dewar region. (Oxygen liquefies at $90.2^{O}K$ at a pressure of one atmosphere and at $82^{O}K$ at 0.387 atmosphere, while

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nitrogen liquefies at $77.347^{\circ}K$ at one atmosphere and $70^{\circ}K$ at 0.381 atmosphere.) Following the onset of liquefication, the chip approaches its minimum temperature. As the gas pressure further decreases, the liquefied gas begins to boil off because the temperature required for liquefication decreases with decreasing pressure. The chip temperature now begins to increase toward the first maximum. At some point as the gas pressure increases, the pressure-temperature conditions required for liquefication are reestablished. Liquefication becomes reinitiated again decreasing the cold finger-to-dewar top cap thermal resistance and the dewar convective heat load, thereby cooling the chip until the second temperature minimum is attained. The process then repeats itself.

Damping out of the temperature excursions, which may be viewed as a successive but decreasing rise in temperature at each temperature minimum, is believed to be due to a thermal time constant associated with cooling down other parts of the dewar. One such part is the dewar glass lead frame to which the top cap is attached. It is noted that the opposite end of the dewar glass lead frame is in contact with the ambient end of the cooler which warms up during cooldown. In run 1-17-11-801 of Fig. 26 a specially constructed forced-air-cooled heatsink was attached to the ambient end. The temperature of the ambient end was $25^{\circ}C$ at the start of the run and rose to $33^{\circ}C$ in ten minutes and held at this temperature for the remainder of the run.

Also listed in Fig. 26 (and in each subsequent cooldown plot) is the leveling-off current of the cooler compressor. The leveling-off current is typically reached within 16 to 20 minutes of the start of cooldown and is a measure of the amount of work being performed by the cooler. With the input voltage held constant, the current initially drawn by the cooler is low, because the cooler is working against a small temperature difference. As the temperature of the cold end decreases, the current increases because more work is being performed. A plot of the current drawn by cooler S/N 013 during its first operation is given in Fig. 27. The current drawn by the cooler is initially 1.5 A and rises to the leveling-off value of 2.8 A in 18 minutes.

The variation in chip temperature with cooldown time during a second run (run 2-18-11-801) is shown in Fig. 28. The same cooler/dewar arrangement used in the preceding run was used. This second run was performed one day later and all other conditions are identical to the preceding run except for a small difference in the leveling-off current and a one-degree centigrade difference in the ambient end temperature which during this second run stablized at $32^{\circ}C$. The difference between the temperature/time behavior of the two runs is not understood. A possibility that cannot be fully discounted is that the O-ring seal of the cryopumped region may have leaked and admitted some air and that water vapor may play a role in the second run.

The manner in which chip temperature varied during a third cooldown run (run 2-18-11-802) in which dry nitrogen gas instead of air was used in the cryopumped region is shown in Fig. 29. Here, the first minimum is also about $73^{\circ}K$ and also attained in about 18 minutes. The first maximum which is reached in 24 minutes is less than $85^{\circ}K$ which is not nearly as large as the first maximum of the preceding two runs. The subsequent temperature excursions are smaller, and it appears that the temperature excursions will eventually dampen out between 82 and $83^{\circ}K$.

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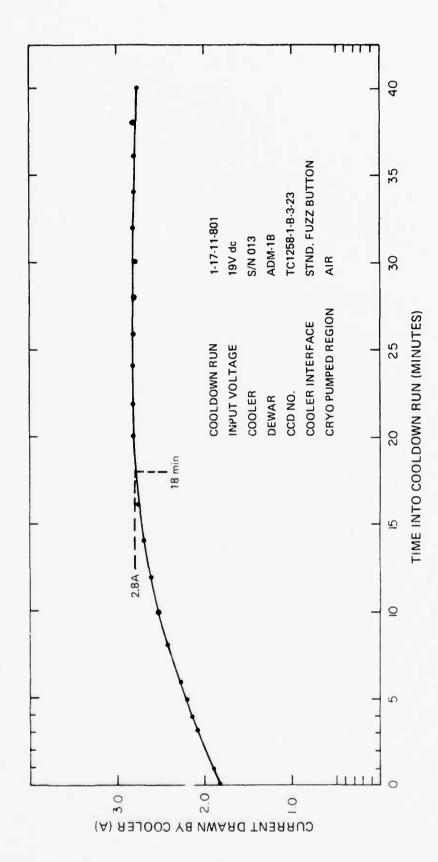Fig. 27. Current drawn by cooler S/N 013 during first cooldown run.
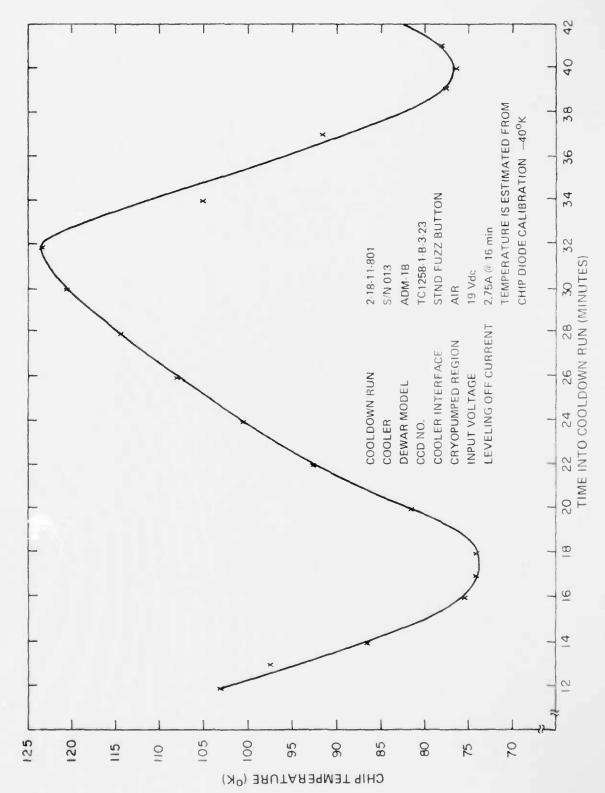
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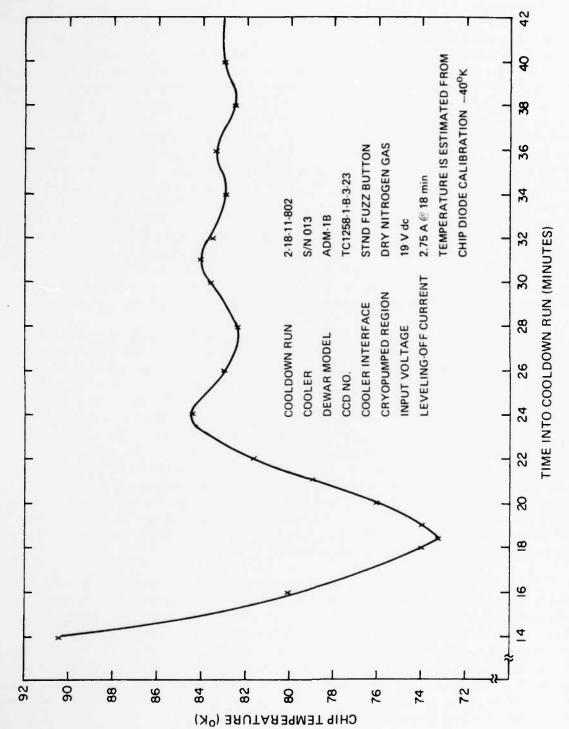Fig. 28. Variation of chip temperature with cooldown time (run 2-18-11-801).

Fig. 29. Variation of chip temperature with cooldown time (dry N_2 gas in cryopumped region of dewar).

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The temperature versus time dependence of the two runs in Fig. 30 indicates that the hard-vacuum region of the dewar also plays a role in the temperature cycling. These runs were carried out before the three preceding runs and were performed specifically for the purpose of determining whether refiring the getter would improve the vacuum and lead to reduced dewar heat load. The cooler used in these runs (runs 4-13-11-801 and -802) was cooler S/N 012, but the dewar was the same model ADM-1B dewar. The two cooldown runs were performed back-to-back and were interrupted only by the time required to refire the getter and to allow the dewar to cool to room temperature afterwards. In the pregetter cooldown, curve "a" of Fig. 30, the minimum temperature was about 71^OK and was reached about 21 minutes into the cooldown run. Following the minimum, the temperature increased, decreased, and increased again. The temperature cycling differs in several respects from the previous cycling in that the periodicity is shorter, the first maximum is only 10^OK greater than the first minimum, and the second maximum exceeds the first. After the refiring of the getter, the minimum temperature reached was about 64^OK after about 24 minutes. The temperature then climbed gradually, and it appears that temperature is starting a longer period temperature cycle. These results show that refiring the getter improved the vacuum and suggests that rapid temperature fluctuations during cooldown are associated with vacuum conditions in the dewar high-vacuum region, whereas the more gradual temperature fluctuations are caused by processes occurring in the cryopumped vacuum region.

The effects of adding acetone to the cryopumped region of the dewar were examined in an effort to improve the thermal interface between the cooler cold finger and the dewar top cap. Two arrangements were used — in one, three drops of acetone were inserted into the standard fuzz button (run 4-20-11-801), and in the second (run 4-20-11-802) three drops of acetone were used in a noncontacting thermal interface. In each case, a small quantity of acetone was also applied over the surface of the inside wall of the glass lead frame. Cooldown plots for the two runs are given in Fig. 31. The most striking feature of these runs is that temperature cycling is not present. It is noted that the times required to attain the minimum temperature (72^OK reached at 28 minutes for run 4-20-11-801 and 76^OK reached at 44 minutes for run 4-20-11-802) are significantly longer than in the other runs suggesting that temperature equilibrium with other parts of the dewar has been reached. The equilibrium temperatures are 75^OK (at 36 minutes) for the case of the acetone impregnated fuzz button and 77^OK (at 44 minutes) for the run using the noncontacting interface and acetone.

The mechanisms by which acetone in the cryopumped region of the dewar affects cooldown are not understood. It is believed that acetone vapors, which condense at a relatively high temperature, freeze to form small thermally conducting filaments between the tip of the cold finger and the dewar top cap, thereby reducing the thermal resistance of this interface. It may also be possible that some of the air is displaced during insertion of the acetone, by the acetone vapor that results during evaporation, and leads to an air/acetone vapor mixture in the cryopumped dewar region. Should this occur, cryopumping would lead to a lower gas pressure and hence to reduced convective heat transfer in the cryopumped region.
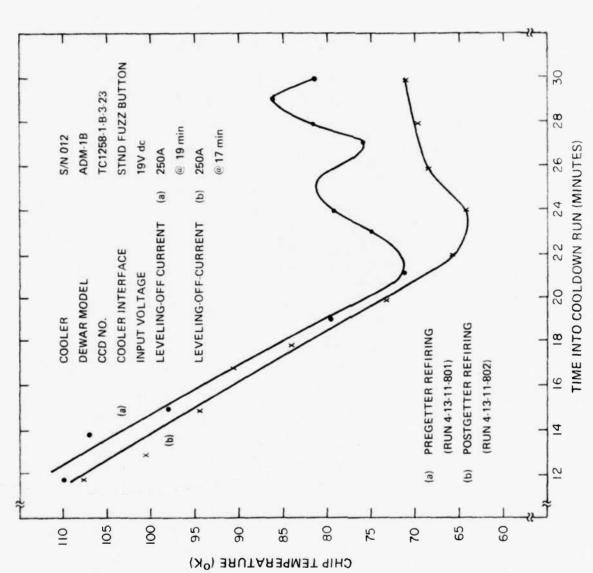
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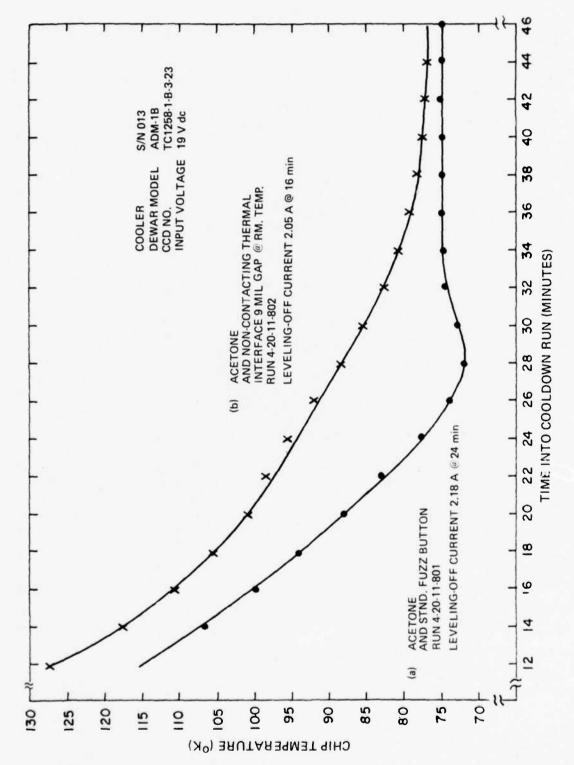Fig. 30. Variation of chip temperature with cooldown time (pre and postgetter refiring).

Fig. 31. Dewar cooldown with acetone in cryopumped region of dewar.

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The results obtained with the acetone impregnated fuzz button (run 4-20-11-801) are encouraging. The minimum temperature of 72°K is the same as the lowest temperature reached during the first cooldown run using cooler S/N 013. During the first cooldown (run 1-17-11-801), the cooler leveling-off current was 2.80 A corresponding to 53.2 W into the cooler whereas during the acetone impregnated fuzz button run, the leveling-off current was 2.18 A for a cooler input power of 41.42 W. Thus, the same minimum temperature was reached even though the input power was about 22 percent less. In subsequent runs, including one which duplicated the first cooler S/N 013 cooldown run, it became clear that the cooler characteristics had changed and that the cooler could not produce the same refrigeration.

A summary of some of the pertinent results of the seven cooldown runs involving the ADM-1B dewar and arranged in chronological order is given in Table 4.

To examine further the question of the temperature required to obtain proper operation of the CCD, the dewar was disconnected from the cooler and liquid nitrogen was poured into it. The use of liquid nitrogen in the dewar maintains the dewar top cap, to which the CCD package is soldered, at 77°K. To the extent that chip power dissipation is negligible and provided the chip-to-package, thermal interface resistance is low enough, the chip should also be at 77°K. (Onchip power dissipation was measured to be about 30 mW as described in Section VI. As may be seen from Table 5, V_{G1T} required to saturate the array under these conditions exceeds 9 V at 12.5 percent and 25 percent integration, but is only +0.01 V at maximum integration. Also, as shown in Table 5, although V_{G1T} could be made equal to 3 V (a value readily realized in other TC1258 CCDs)[3] the dark level plus background exceeds 70 percent of the saturation level, leaving only 30 percent dynamic range.

In view of the experience with CCD TC1258-1-B-3-23 in the ADM-1B dewar, it appears that even at 77°K the array is not cold enough to operate properly; or the array is much warmer than is thought; or the particular CCD exhibits larger dark leakage current than others.

A tabulation of all of the cooldown runs attempted to date (19 runs) which include results with the model Y dewar (an actively pumped dewar), the model ADM-1A (a sealed dewar having a soft vacuum and an inoperable CCD), and the model ADM-1B dewar is given in Table 6. The seven runs for which temperature versus time plots are given are identified by asterisks.

The last tabulated run (run 5-21-11-802) in Table 6 relates to an attempt to reproduce the results of the first run using cooler S/N 013 (run 1-17-11-801) and shows that the cooler's cooling capacity has drastically diminished. A plot of the cooler current versus time for run 5-21-11-802 given in Fig. 32 shows that the current at the start of cooldown was only 1.5 A and that the leveling-off current reached only 1.85 A.

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TABLE 4. SUMMARY OF PERTINENT RESULTS OF SEVEN SELECTED COOLDOWN RUNS

Run Number	Description Run	Cooler[a] Number	Cooler Leveling-Off Power (Watts)	Lowest Temperature Attained ($^{\circ}$K) & (Time)	Temperature Cycling	Temperature at End of Run ($^{\circ}$K)
4-13-11-801	Pregetter Refiring Stnd. Fuzz Button,[b]Air	S/N 012	47.5	71°K (21 min)	Yes	83°K (35 min)
4-13-11-802	Postgetter Refiring Stnd. Fuzz Button, Air	S/N 012	47.5	64°K (24 min)	appears that will cycle	71°K (30 min)
1-17-11-801	First Cooldown S/N 013 Stnd. Fuzz Button, Air	S/N 013	53.2	72°K (18 min)	Yes	85°K (50 min)
2-18-11-801	Cooldown in preparation to lens alignment Stnd. Fuzz Button, Air	S/N 013	52.25	74°K (17 min)	Yes	82°K (42 min)
2-18-11-802	Run with Dry N2; Stnd. Fuzz Button, Nitrogen	S/N 013	52.25	73°K (18.5 min)	Yes	83°K (42 min)
4-20-11-801	Acetone and Stnd. Arrangement; Stnd. Fuzz Button, Air	S/N 013	41.42	72°K (28 min)	No	75°K (46 min)
4-20-11-802	Acetone & Noncontacting Thermal Interface. 9-mil gap at Rm. Temp.[c]	S/N 013 S/N 013	38.95 38.95	77°K (42 mi)	No	77°K (46 min)

(a) Coolers - 1 watt split cycle, Tri-Service Common Module Cooler

(b) Stnd. Fuzz Button - 0.125 in x 0.560 in diameter

(c) Gap at 77°K estimated to be 13 mils; 1.4 gm copper extender on cold finger applied with thermal grease

ALL RUNS: ADM-1B Dewar; V_{in} = 19 V dc

TABLE 5. V_{G1T} AT WHICH ARRAY OUTPUT SATURATES AND ARRAY
OUTPUT AT SELECTED VALUES OF V_{G1T} AT 77^OK

(a) V_{GIT} to Saturate at 77^OK

Integration step	V_{G1T} at which array output is saturated (V)
Max.	+0.01
50%	+0.77
25%	>9
12.5%	>9

(b) Array Dark and Background Output at Selected V_{G1T} at 77^OK

Integration step	V_{G1T}(V)	Dark level plus background as percent of saturation (%)
Max.	-0.01	89.5
50%	+0.45	82.0
25%	+3.00	82.0
12.5%	+3.00	71.6

Maximum integration = 109.27 ms

Array saturation = 3.35 V

CCD No. TC1258-1-B-3-23

Run No. 5-21-11-80LN2

ADM-1B dewar, top cap held at 77^OK with liquid nitrogen

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TABLE 6. TABULATION OF ALL COOLDOWN RUNS

Run No.	Cooler S/N	Dewar Model	CCD No. TCI258	Description of Run	Input Voltage (V)	Leveling-Off Current (A)	Temperature (°K)	Temp. Cycling	Comments
5-19-09-s01	009	Y	-1-J2-24	Checkout of Model Y Dewar	18 V	2.70	72°K[a] (45 min)	No	Dewar actively pumped
5-24-10-s01	012	ADM-1A	-1-J3-9	Checkout of ADM-1A Dewar	19 V	2.25	175°K (14 min)	No	Dewar soft, cooler current erratic and cooler noise
4-6-11-s01	012	ADM-1B	-1-B-3-23	Checkout of ADM-1B Dewar	19 V	2.65	57°K (26 min)	Yes[b]	cooler current erratic and cooler noise
1-7-11-s01	011	ADM-1B	-1-B-3-23	First operation of cooler S/N 011	19 V	3.0	—	—	current dropped from 3.0 to 2.0 A
2-11-11-s01	014	ADM-1B	-1-B-3-23	First operation of cooler S/N 014	19 V	3.10	73°K (22 min)	Yes[c]	
4-12-11-s01	014	ADM-1B	-1-B-3-23	Standard-fit Fuzz Button (ht. 0.125 in)	19 V		67°K (21 min)	Yes	
4-12-11-s02	014	ADM-1B	-1-B-3-23	Reduced-fit Fuzz Button (ht. 0.100 in)	19 V	2.82	71°K (22 min)	Yes	only run with reduced ht. fuzz button
4-13-11-s01	012	ADM-1B	-1-B-3-23	Pregetter Refiring	19 V	2.50	71°K (21 min)	Yes	cooler current not erratic no unusual noise
4-13-11-s02	012	ADM-1B	-1-B-3-23	Postgetter Refiring	19 V	2.50	61°K (21 min)	—	appears unit will cyclr
4-13-11-s03	014	Y	-1-J2-24	Attempt to duplicate run 5-19-09-s01 with cooler S/N 014	19 V	2.75	102°K (20 min)	Yes	suspect poor vacuum
4-17-11-s01	013	ADM-1B	-1-B-3-23	1st operation of cooler S/N 013	19 V	2.80	72°K (18 min)	Yes	
2-18-11-s01	013	ADM-1B	-1-B-3-23	Cooldown in preparation for lens alignment	19 V	2.75	71°K (17 min)	Yes	
2-4-11-s02	013	ADM-1B	-1-B-3-23	Dry N2 (1st)		2.75	73°K (18.5 min)	Yes	
3-19-11-s01	013	ADM-1B	-1-B-3-23	First attempt to operate system with IR diodes biased on at outset	19 V	2.60	77°K (20 min)	Yes	Dry N2 in dewar
4-20-11-s01	013	ADM-1B	-1-B-3-23	Acetone and Std. Fuzz Button	19 V	2.18	72°K (28 min)	No	
4-20-11-s02	013	ADM-1B	-1-B-3-23	Acetone and large gap d-mils noncontacting thermal interface	19 V	2.05	74°K (14 min)	No	
4-20-11-s03	013	ADM-1B	-1-B-3-23	Acetone and small gap d-mils noncontacting thermal interface	19 V	2.0	84°K (51 min)	No	
5-21-11-s01	013	ADM-1B	-1-B-3-23	No material between tip of cooler cold finger and dewar top plate (71-mil gap)	19 V	1.90	100°K (50 min)	No	
5-21-11-s02	013	ADM-1B	-1-B-3-23	Attempt to repeat run 4-17-11-s01	19 V	1.85	105°K (56 min)	No	Cooler capacity has dropped

[a] Onchip diode not calibrated but lowest temp is 9mV less than with LN2 in dewar

[b] Amplitude of cycling small, less than 2°K.

[c] First max. approx. 5°K higher than min.

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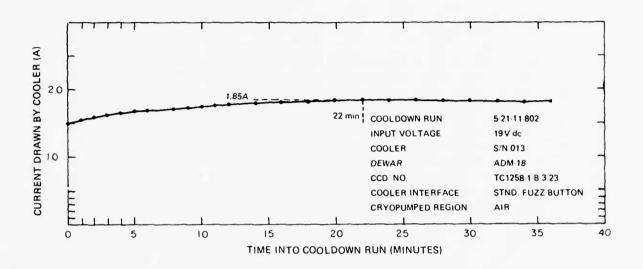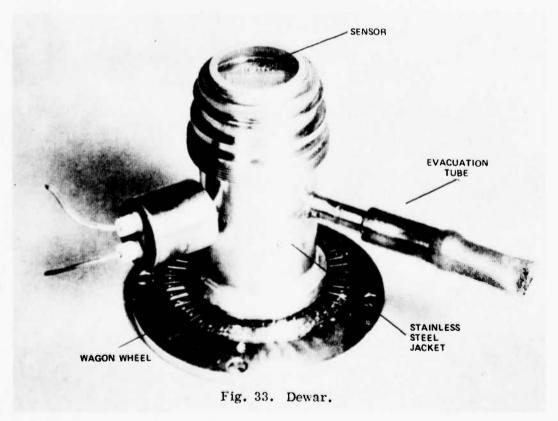
Fig. 32. Current drawn by cooler S/N 013 following use of the cooler in eight prior cooldown runs.

Section VI

DEWAR FABRICATION AND THERMAL MEASUREMENTS

A. DEWAR FABRICATION

Several modifications in dewar assembly were made to avoid the mechanical reliability problems encountered with the glass wagonwheel feedthrough (Figs. 33 and 34). The metal preparation in the glass-to-metal seal was inadequate (as discussed in the Second Interim technical report). The wagonwheel feedthroughs were remanufactured with the metal surfaces sand-blasted and oxided more heavily. This greatly improved the mechanical strength of the seal. Stresses are induced in the glass due to the difference in the coefficient of thermal expansion between the Kovar in the wagonwheel and the stainless steel in the outer cylinder. The outer cylinder is soldered (see Fig. 35) to the wagonwheel in the last assembly step prior to pumpout. Soldering is used so that the dewar may be reopened if necessary. When this joint is made, the parts are heated to a few degrees above the melting point of the solder. The solder sets as the parts cool. Stainless steel contracts about three times more than the Kovar which stresses the parts at room temperature. This stress was calculated to be 3,900 PSI, which exceeds the allowable working stress of 1,600 PSI for type 7052 glass in the wagonwheel feedthrough. Therefore, the material for the outer cylinder was changed to Kovar. Leak testing of the Kovar is planned after machining.

Fig. 33. Dewar.

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Fig. 34. Dewar components.

Fig. 35. Dewar fabrication.

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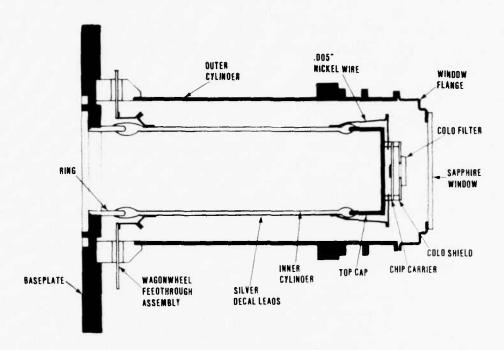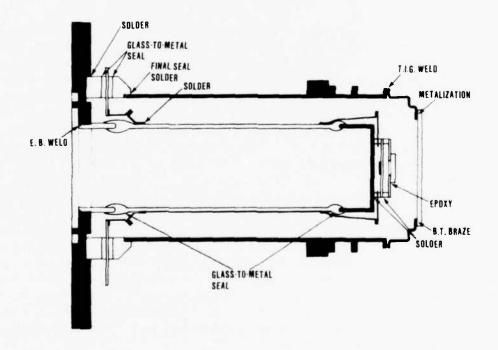As a short term solution to the wagonwheel breakage problem, a dewar was constructed (model Y) using epoxy instead of solder. Because the vacuum integrity of the model Y dewar would be questionable, the dewar was actively pumped while testing. This dewar contains an electrically operative CCD and was used for testing until a sealed dewar was completed.

The first ADM-1 dewar containing a potentially operable CCD (called the ADM-1A dewar and containing CCD TC1258-1-J-3-9 obtained from RADC/ET on 8 August 1980) was assembled. However, upon retesting (electrical inputting at room temperature to verify the predewar assembly operation of the CCD), it was found that the CCD was no longer operable. The CCD could not be electrically inputted, the output was independent of "fat zero," and the standard pixel output waveform was greatly distorted. A cooldown test of the ADM-1A dewar was then performed using cooler S/N 012. After 16 minutes of operation, it became apparent that the dewar vacuum was soft. The outside of the dewar felt cold to the touch after a few minutes of operation and the temperature, as measured by the onchip temperature sense diode, bottomed out near $175^{O}K$ after approximately 12 minutes.

The ADM-1 dewar had been reworked a number of times, and it is believed that the failure of the CCD can probably be attributed to the large amount of rework. The cause of the failure of the dewar was identified as being a defective pinchoff of the copper evacuation tube. However, the use of a low-melting-temperature indium solder and a vacuum sealant to join the stainless-steel dewar outer wall to the Kovar section of the wagonwheel lead-frame connector proved to be effective.

The parts of the ADM-1A dewar were then used with the second potentially operable CCD in an attempt to make another dewar for ADM-1. The CCD used in this second dewar, called the ADM-1B dewar, is the TC1258-1-B-3-23, which was obtained also from RADC/ET on 8 August 1980. The CCD was tested at room temperature with electrical inputting and its onchip temperature sense diode was calibrated (in the Lake Shore refrigerator with a Lake Shore diode) before committing the CCD to the dewar assembly process. Between $100^{O}K$ and $50^{O}K$, the diode output at 10.27 microamperes was almost linear with a slope of 2 mV/^{O}K. Between room temperature and $100^{O}K$ the slope was about 2.48 mV/^{O}K.

Following soldering of the CCD into the ADM-1B dewar and assembly, bakeout, and pumpdown of the dewar, the CCD was retested at room temperature. The test indicated the CCD to be operating properly and with no detectable change over the predewar assembly test. A cooldown of the ADM-1B dewar with cooler S/N 012 was then performed, and it was found that the calibration of the onchip temperature sense diode no longer applied. The diode voltage, which previously had been -0.580 V at room temperature was -0.518 V indicating a difference of $25^{O}K$. The reason for this discrepancy is not known. The minimum temperature attained with cooler S/N 012 was about $13^{O}K$ colder than with the CCD mounting flange held at $77^{O}K$ with LN_2 (-1.048 V with cooler versus 1.022 V with LN_2 and 2 mV/^{O}K).

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B. THERMAL MEASUREMENTS

Due to the difficulties encountered in reaching acceptably low CCD temperatures in ADM-1B and Y dewars when operated with the coolers (discussed in Section IV), the dewar heat load was investigated. The standard method of measuring the heat load of a dewar is the liquid nitrogen boiloff test. In this type of measurement, it is assumed that all of the heat energy into the dewar is expended in the heat of vaporization of the nitrogen. The measurement is conducted by filling the cold finger area of the dewar with LN_2 and measuring the flow rate of nitrogen gas from the dewar with a linear mass flow meter (Tylan model FM200, 100 SCCM range); the arrangement of the test setup is shown in Fig. 36. The output of the flow meter is recorded on a strip chart recorder. The results of a typical test are shown in Fig. 37. As the liquid level drops, the boil-off rate decreases because the effective length of glass wall between the surface of the liquid and the ambient end of the dewar is increasing. As the effective length increases, the thermal resistance increases. Just before the last nitrogen has boiled off, the liquid is contained totally in the top cap. Because the top cap is metal, the thermal resistance is essentially constant at this point. This can be seen in Fig. 37 as the point where the curve levels off immediately prior to the end of the test. The value where the flow rate levels off is used to find the heat load. The measurements have been repeatable to 3 percent over four trials on two different days. The ADM-1B dewar measured 267 mW heat load, and the model Y dewar was 397 mW. The higher load of the model Y is caused by at least two factors. The model Y has lower resistance silver decal leads, and the pump used on the model Y does not reach as low a pressure as the sealed-off dewar.
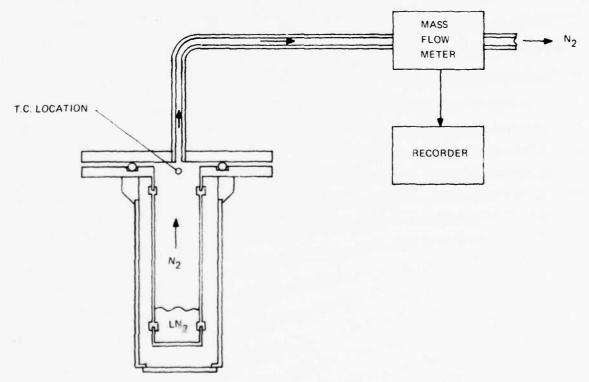

Fig. 36. Arrangement used in liquid nitrogen boiloff test to determine dewar heat load.
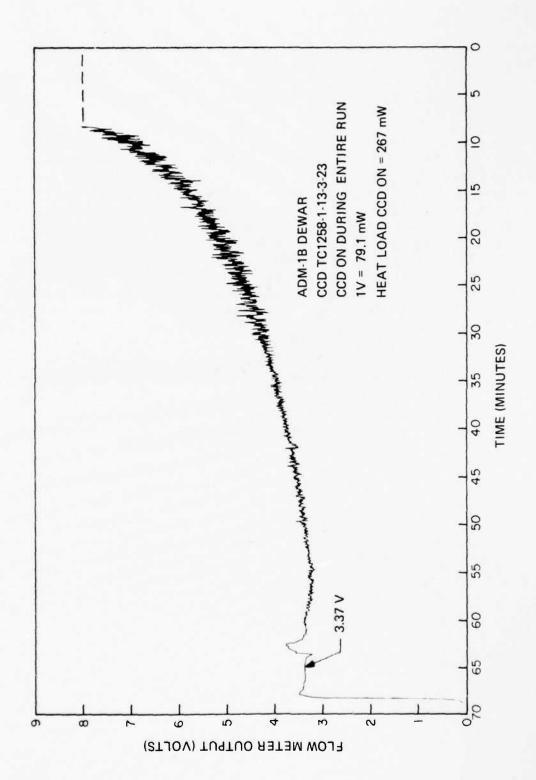
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Fig. 37. Flow meter output vs. time during a liquid nitrogen boiloff test of dewar ADM-1B with CCD operating.

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Although the ADM-1B dewar boiloff test indicated a low heat load, our operating experience indicated that it might actually be higher. Upon later examination of the boiloff test, it appeared that there may be inaccuracies in this method. The saturated liquid nitrogen changes to a saturated vapor and absorbs heat. However, the 77°K nitrogen vapor passes along the glass inner wall, removing additional heat. To find the magnitude of this effect, a thermocouple was placed in the gas stream at the exit of the dewar. If the gas was at 77°K, then the original heat load measurement is accurate. The result was that the gas was 275°K. Therefore, heat was being removed from the dewar to raise the gas temperature from 77°K to 275°K. This results in 253 mW additional heat load, for a total of 520 mW for the ADM-1B. These results were discussed with Ron Woodard of Martin-Marietta who supplied the one-watt coolers. He has found an empirical rule-of-thumb where the actual heat load is two times the value obtained in a liquid nitrogen boiloff test. This agrees with our experiments.

In operation with a cooler, the baseplate of the dewar stabilizes at 28°C. This elevated temperature is caused by the heat rejected from the ambient end of the cooler cold finger. In a boiloff test, however, the nitrogen vapor leaving the dewar cools the baseplate to 17°C. Thus, to more closely model operation with a cooler, a resistance heater and thermocouple were mounted on the baseplate to maintain 28°C throughout the boiloff. The elevated temperature raised the heat load by only 6.3 mW (397.1 mW at 17°C, 403.4 mW at 28°C). Therefore, it was concluded that this effect can be neglected.

The boiloff test was used to measure the heat dissipation of the CCD. At the start of the test, no power was applied to the CCD. When the heat load leveled off, a measurement was recorded, the CCD power was applied, and the heat load increase was noted. The CCD power was switched off again to verify the first measurement. The data for the run is shown in Fig. 38.

Using the model Y dewar, measurement was made of the temperature drop across the fuzz button interface. Thermocouples were mounted on the tip of the cold finger and on the surface of the top cap. The interface ΔT across a standard-height fuzz button was 6°C.
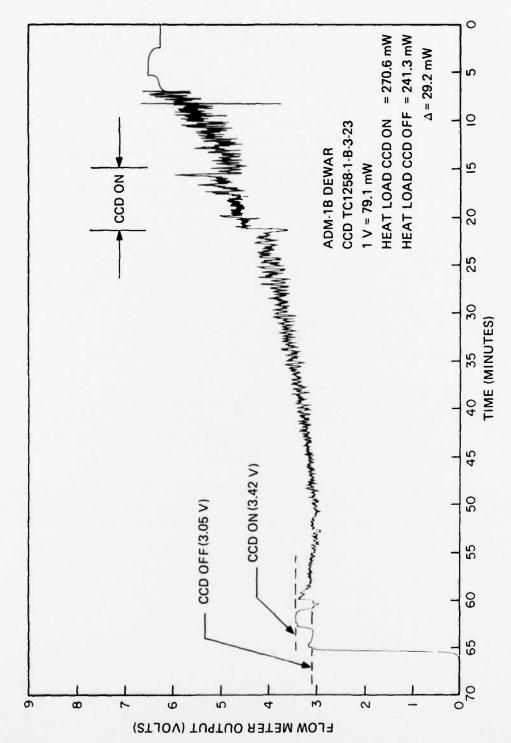
Fig. 38. Flow meter output vs. time during a liquid nitrogen boiloff test of dewar ADM-1B showing power dissipation by CCD.

ADM-1B DEWAR
CCD TC1258-1-B-3-23
1 V = 79.1 mW
HEAT LOAD CCD ON   = 270.6 mW
HEAT LOAD CCD OFF = 241.3 mW
Δ = 29.2 mW

CCD OFF (3.05 V)
CCD ON (3.42 V)

CCD ON

FLOW METER OUTPUT (VOLTS)
TIME (MINUTES)

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Section VII

SIGNAL PROCESSOR

A description of the signal processor for ADM-1 was given in the Second Interim Report. Testing of the software used in ADM-1 has illustrated the need for revision in the threshold determination area. The software that was exercised in the testing phase was contained in EPROM set 6.

The ADM-1 signal processor (EPROM set 6) used a noise model that was similar to that proposed by Purdue University.[4] It is a background noise model and is given by equation 1.

$$b = d \left(\frac{N+1}{N} \right)^{1/2} \left(M_\ell \right)^{1/2} \tag{1}$$

where b = decision threshold
N = number of samples used in background time average
M_ℓ = background time average
d = scaling factor

This noise model (Fig. 39) is accurate if the CCD and is connected to the micro-processor via A/D converter, i.e., the system gain is equal to one.
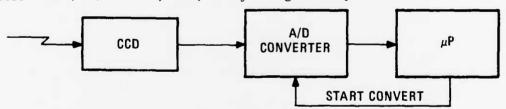

Fig. 39. Basic system configuration.

The introduction of an automatic level control system to extend the sensor's dynamic range results in the system configuration given in Fig. 40.
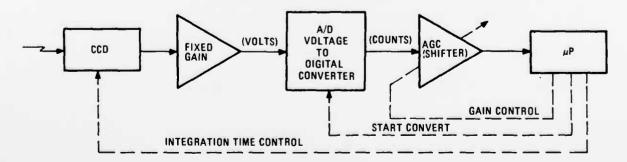

Fig. 40. System configuration with automatic level control.

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The addition of the automatic level control system forces a modification in the decision threshold equation because the system gain is no longer equal to one. In fact, the automatic gain control circuit, the digital shifter in Fig. 40, can have four different gain settings. There is also a fixed-gain component introduced to enhance the CCD drive capability and to match the output amplitude of the CCD to the input range of the analog-to-digital converter. This fixed gain component can be included in the scaling factor "d". But the basic decision threshold model must be modified to reflect the addition of the variable gain component. A derivation and interpretation of a modified decision threshold equation follows.

The background noise model proposed by Purdue is referenced at the output of the CCD and is stated in equation 2 in volts.

$$b_v = d \left(\frac{N+1}{N}\right)^{1/2} \left(\frac{B_v\, q}{C}\right)^{1/2} \tag{2}$$

where B_v = BTA in volts at CCD output

C = output capacitance of CCD

q = charge of an electron

N = number of samples used in BTA

d = scaling factor

b_v = decision threshold in volts at CCD output

However, the signal arriving at the input of the microprocessor has been multiplied by the system gain. Thus, for the microprocessor to reference the background time average to the output of the CCD, it must divide the BTA by the system gain.

$$b_v = d \left(\frac{N+1}{N}\right)^{1/2} \left(\frac{B_v'\, q}{A_v\, G_{shft}\, C}\right)^{1/2} \tag{3}$$

where A_v = fixed system gain

G_{shft} = AGC gain due to shifter

B_v' = BTA in volts at microprocessor

Equation 3 yields the decision threshold as referenced to the output of the CCD. To reference the decision threshold to the input of the microprocessor, the decision threshold at the CCD must be multiplied by the system gain.

$$b_v' = A_v\, G_{shft}\, b_v \tag{4}$$

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$$b_v' = A_v \, G_{shft} \, d \left(\frac{N+1}{N}\right)^{1/2} \left(\frac{B_v' \, q}{A_v \, G_{shft} C}\right)^{1/2} \tag{5}$$

where $\quad b_v' = $ decision threshold referenced at the microcomputer

$$b_v' = d \left(\frac{N+1}{N}\right)^{1/2} \left(A_v \, G_{shft}\right)^{1/2} \left(\frac{B_v' \, q}{C}\right)^{1/2} \tag{6}$$

If the fixed system gain is incorporated into the scale factor constant d, and because $\frac{B_v \, q}{C}$ equals the background time average in volts squared, equation 6 reduces to the following:

$$b_v' = d_1 \left(\frac{N+1}{N}\right)^{1/2} \left(G_{shft}\right)^{1/2} \left(BTA\right)^{1/2} \tag{7}$$

where $\quad d_1 \quad$ = adjusted scale factor

$\quad$ BTA = background time average = $\dfrac{B_v' \, q}{C}$

Equation 7 is the one used to determine the decision threshold in EPROM set 8.

EPROM set 6 (the tested set) did not take into account the effect of the automatic gain control, G_{shft}. The automatic gain control is binary in nature and hence takes on values 1, 2, 4, and 8. Thus, the resulting threshold determination was in error by the square root of the automatic gain control value. The following errors for threshold as determined by EPROM set 6 are presented in Table 7.

TABLE 7. THRESHOLD ERRORS

Integration Mode (%)	AGC Value	Threshold Error
100	1	None
50	2	1.414
25	4	2
12.5	8	2.828

The error introduced by not taking the AGC setting into account was partially masked by the threshold correction factor, TCF, mechanism discussed in the Second Interim Report and is nonexistent when operating in the maximum integration mode.

The correction of the AGC error involves the use of four BTA/threshold curves as opposed to the one used in the EPROM set 6 approach. This means at the start of the threshold determination the current setting of the gain in the AGC circuit must be determined by the processor to select the proper BTA/threshold curve.

The BTA value should be independent of the integration mode selected. The input signal for a fixed scene theoretically does not depend on the AGC setting because of the inverse relationship between integration time and AGC gain. For example, when the integration time was doubled, the shifter gain was cut by one-half. The integration time increase should result in twice as much signal from the CCD because the chip accumulated charge for twice the time period. However, before the signal is presented to the processor, the shifter (digital gain stage) divides the CCD output signal by two. Thus, the signal to the processor is the same in both integration modes. It follows that the BTA is also the same in both integration modes. This approach should ensure the orderly transition between integration modes without issuing an intrusion alarm.

The background time average is used in conjunction with the appropriate BTA/ threshold table and index table value to determine the decision threshold. A binary tree search approach (see Fig. 41) is used to determine decision threshold. The index table consists of a list of the binary delta increments. A binary delta increment is the offset address of the mid, one-fourth, and one-eighth points of the BTA threshold table. Thus, when the binary delta increment is added to the start address of the BTA/threshold table, it identifies the 1/2, 1/4, 1/8, etc. points contained in the table. For example, if the BTA/threshold table contains 256 values, the first delta increment in the index table (1/2) would be 128 and the second delta increment (1/4) would be 64. An index table for a 256-value BTA/threshold case is given in Table 8.

TABLE 8. DELTA INCREMENT VALUES

Contents	Value
1/2	128
1/4	64
1/8	32
1/16	16
1/32	8
1/64	4
1/128	2
1/256	1

The delta increment values are calculated in nonreal time. The number of index values depends on the number of values in the BTA/threshold reference table which is a function of the operating parameters. The number can be calculated by taking the log base 2 of the number of values in the BTA/threshold reference table and rounding off the result to the next highest integer. This integer value plus one is the number of searches that must be performed to determine the decision threshold.
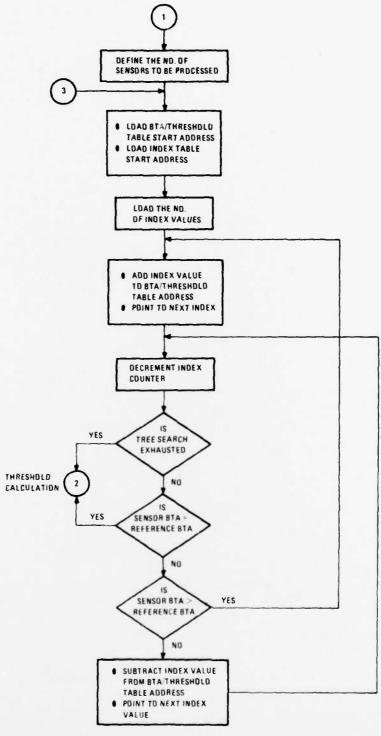
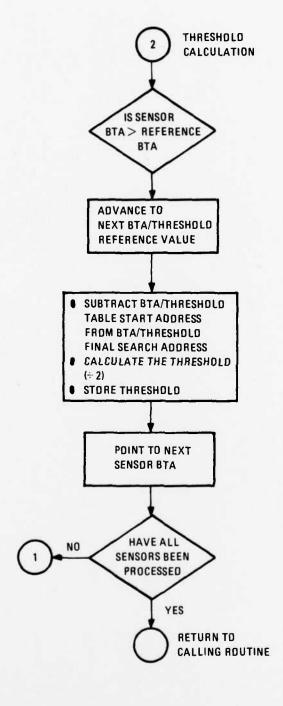Fig. 41. Binary tree search approach (sheet 1 of 2).

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Fig. 41. Binary tree search approach (sheet 2 of 2).

The index values are added or subtracted to the current BTA/threshold table address as a result of the comparison of the sensor BTA and the reference table BTA. The index adding/subtracting process is continued until the sensor BTA is found equal to the reference BTA value or until all index values have been used. If in the final comparison the sensor BTA is less than the reference BTA, then the reference BTA is used. If it is not, the next higher reference BTA is used for the threshold calculation. It is this rounding to the highest integer process that inhibits the multiplying or dividing of the existing threshold by the square root of two upon an integration mode change. The binary tree search takes approximately 65 ms to determine the decision threshold for 256 sensors. Because the time required to initialize the Lossy integral and determine the thresholds of 256 sensors exceeds the available line time, 109 ms, two line times will be required to perform the background and threshold initialization. In the 256th line, the Lossy integral will be initialized, but the thresholds will not be computed until the 257th line time (see Table 9 for execution times). No intruder detection processing will be done on the 257th input data.

TABLE 9. EXECUTION TIMES

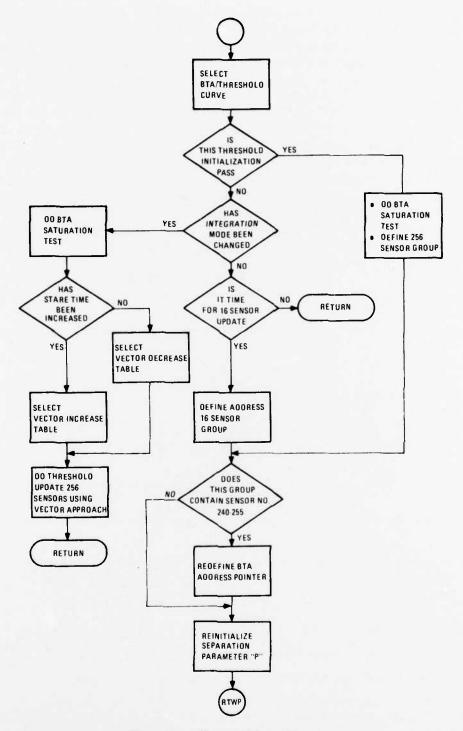| 256th Line	
Subroutine	Execution Time (ms)
● Load	19.304
● Spatial Average	1.037
● External Input Source Select	0.054
● External Data Source Load	0.032
● Lossy Integral Initialization (BTA)	51.560
TOTAL	71.987
257th Line	
Subroutine	Execution Time (ms)
● Load	19.304
● Spatial Average	1.037
● External Input Source Select	0.054
● External Data Source Load	0.032
● Threshold Initialization	64.560
TOTAL	84.987

Fig. 42. Threshold routine.

A. BTA SATURATION TEST

The integration mode is controlled by 16 or 32 spatially separated sensors. If the average value of the spatially separated sensors is less than the lower spatial average limit, the integration time is increased for the entire array. This means that the signal from every sensor should be doubled. The background time average stays the same as a result of a decrease in gain through the automatic gain control system (shifter). A problem arises, however, if one or more sensors has a signal and consequently a BTA value in a fixed scene greater than the maximum possible input count for the integration mode being stepped to. In the new integration mode, the sensor would demand an output value that would be in excess of the possible output from the 12-bit A/D converter (4095) to yield the same background time average as the previous integration mode. The system would respond to the reduced input signal by yielding an alarm condition until the background time average caught up to the new signal input. To remedy this A/D converter saturation problem, the BTA of every sensor is tested to see if it is greater than the maximum possible BTA for the new integration mode. If it is greater, then the BTA for the offending sensor it is forced to the maximum value, saturated. The threshold for the offending sensor is also forced to the corresponding maximum value. Thus, the signal processing parameters for the sensor are forced to the maximum allowable via the processor, but this should not degrade the performance because the sensor channel is saturated as a result of the mode change. The actual gain, however, is the elimination of the false alarm due to the saturated A/D converter. The BTA saturation test for 256 sensors requires 8.7 ms to execute.

B. THRESHOLD ROUTINE

The threshold routine depicted in Fig. 42 consists of five basic parts:

- Decision threshold curve selection

- BTA saturation test

- Binary tree search for initial threshold of 256 sensors

- Threshold maintenance for 16 sensor groups

- Threshold update for 256 sensors using vector approach used after integration mode change.

Each of these areas have been explained in the previous sections. The basic reason for two-decision threshold lookup approaches is a result of the time required for execution. The binary approach uses no a priori knowledge of the sensor threshold and consequently must perform the largest number of comparisons before isolating the decision threshold. The vector update approach utilizes the previous threshold to reduce the amount of searches required to find the decision threshold. Thus, the binary tree search approach is used on threshold initialization where no previous thresholds are

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available and during routine threshold maintnenace. The execution time used in threshold maintenance is kept small by updating only 16 sensors. The execution time approximations are found in Table 10.

TABLE 10. APPROXIMATE EXECUTION TIMES

Subroutine	256 Sensor initialization	16 Sensor Maintenance	Mode Change Update
Threshold Curve Selection	81.9 μs	81.9 μs	81.9 μs
First Pass Test	7.99 μs	7.32 μs	7.32 μs
Integration Mode Change Test	—	31.97 μs	31.97 μs
BTA Saturation Test	8.7 ms	—	8.7 ms
Threshold Update	—	—	18.08 ms
Threshold Maintenance	64.47 ms	4.077 ms	—
TOTAL	73.26 ms	4.198 μs	26.90 ms

The vector update table, the delta increment table, and the four BTA threshold curves are calculated in nonreal time at the start of the program execution.

REFERENCES

1. "IRCCD Fence Sensor System", 2nd Interim Technical Report, Contract F19628-79-C-0026, December 1980.

2. W.F. Kosonocky et al., "256-Element Schottky-Barrier IR-CCD Line Sensor", RADC-TR-77-304, Final Technical Report, September 1977.

3. R. Taylor, Deputy for Electronics Technology, Rome Air Development Center, Hanscom AFB, MA 01731 (private conversation).

4. G.R. Cooper and C.D. McGillem, "IRCCD Intrusion Detection", Purdue University, RADC Technical Report 77-435, October 1978.

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